A Reliable Data Processing for the front-end electronics of the Hyper-Kamiokande Experiment

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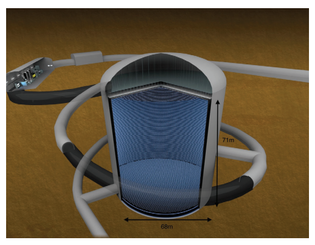
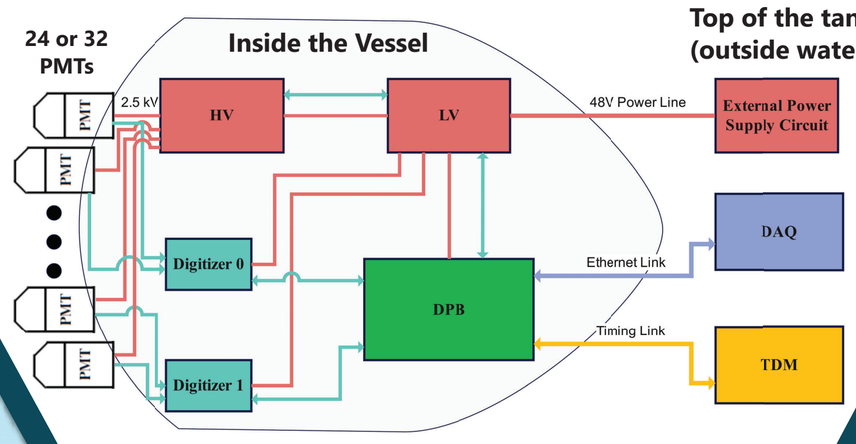
The HK Far Detector

Objectives

1. **CP-Violating Phase** derived from neutrino and antineutrino asymmetries
2. **Mass hierarchy**
3. **Astrophysical neutrinos**
4. **Nucleon decay searches**



Electronics Overview



HK Far Detector Front-end Electronics

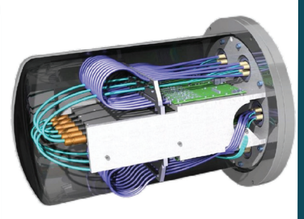
- High Voltage 2.5kV 500uA Board
- Low Voltage 48V to 12V Power Supply
- Digitizer Boards (x2)
- **Data Processing Board**

The Vessel

Hyper-Kamiokande Far Detector Vessel

Watertight pressure-resistant stainless steel vessel

- Custom data / clock / power / gas connection
- Custom PMT feed-throughs



Requisites

Challenges

- **Length of the wires** → twice as long than Super-Kamiokande, from 70m to ~140m
- **Signal interference** → higher probability of signal interference between cables
- **Amount of data** → 20,000 PMTs (ID + OD sides) 4 times the Super-Kamiokande PMTs
- **PMT Support Structure** → new PMTs require a much sturdier support structure

Consequence

Electronics must be placed underwater next to the PMTs!!! Replacement and repairability becomes difficult

Digitizer to DPB Data Rate

$$Rate_{Dig-DPB} = Bph \cdot HR \cdot N_{ch} = 12\frac{Bytes}{Hit}\cdot 1.5\frac{MHit}{s}\cdot 12 = 206\ MiB/s$$

Memory size for event buffering

$$S_{buffer} = Rate \cdot N_{dig} \cdot t_{buffer} = 206\,MiB/s \cdot 2 \cdot 10s = 4\ GiB$$

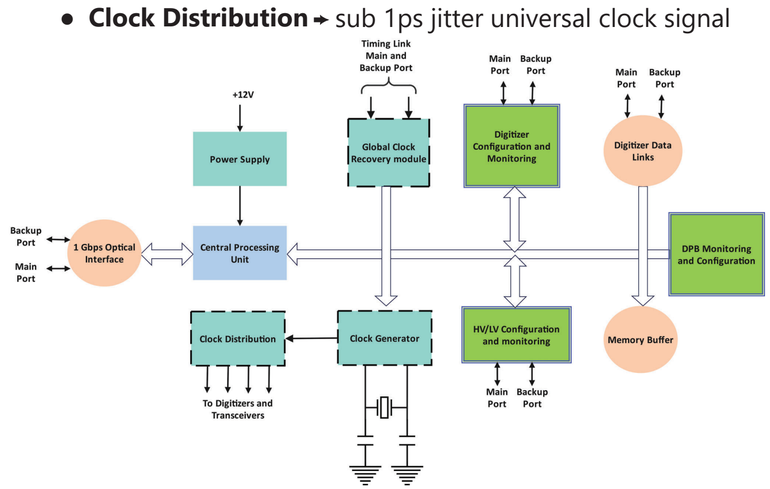
Feature description	Requirement
Digitizer-DPB Link Speed	> 1.4 Gbps
Memory Buffer	> 4 GiB
DPB-DAQ Link Speed	1 Gbps
DPB-Timing Link Speed	125 Mbps
Buffer size	5-10 seconds
Slow Control Period	Include commands to configure any parameter of the FEE
Power Consumption	<15 W nominal
Lifetime	10-20 years with 1% of failure rate

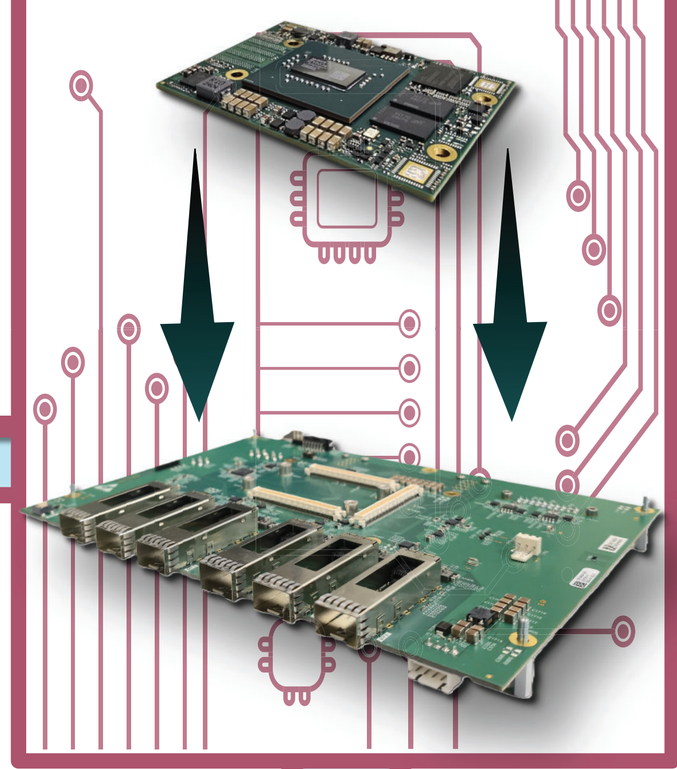
Design Architecture

Functionality

Hub Board that acts as a data aggregator and director of the vessel electronics

- **Central Processing Unit** → management and control unit for the rest of the DPB blocks
- **Data Buffering** → supernova events produce data at higher rates than the DPB-DAQ uplink. Buffering few tens of seconds (worst case scenario) is required to avoid data loss
- **Slow control tasks** → DPB manages the communication to to each board providing a standard interface to the DAQ
- **Clock Distribution** → sub 1ps jitter universal clock signal

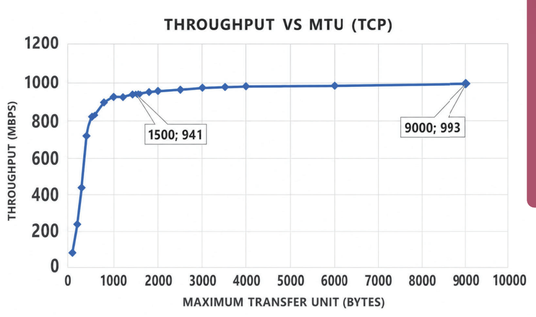




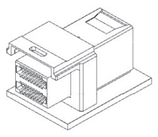
Data Links

Upstream link

- Data connection to DAQ Readout Units
- 1000-BaseX Multimode Fiber
- 2x Redundant Active Backup Links
- Jumbo Frames Support



Downstream link

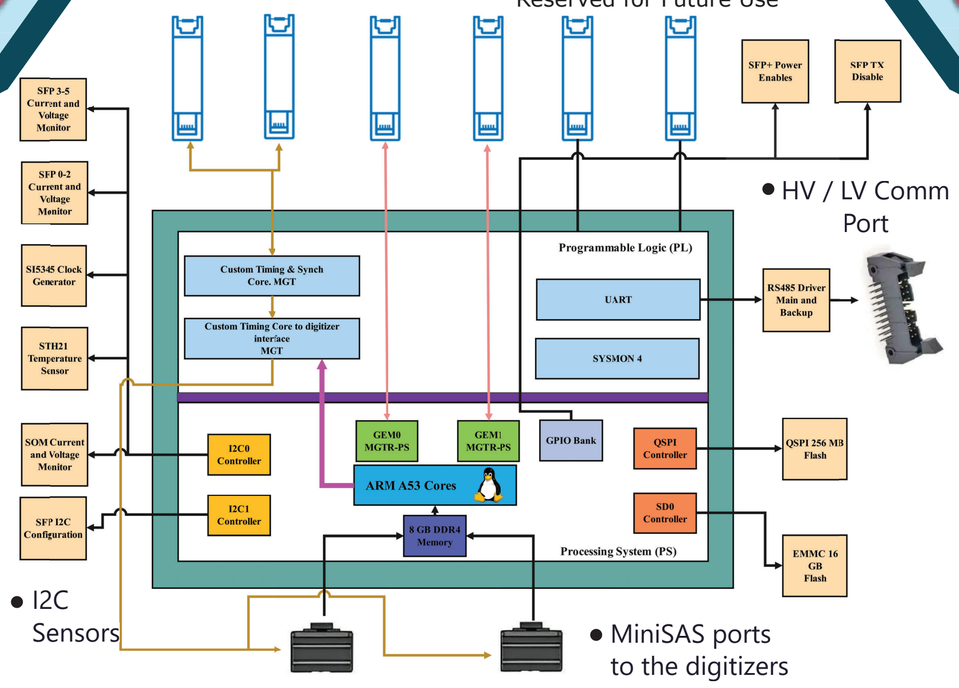


MiniSAS HD SF8643

- Full-Duplex Aurora protocol at 3.125Gbps
- 2x Redundant links for data, clock and timing protocol
- JTAG chain and slow control serial link

SoC (CPU + FPGA Architecture)

- AMD Zynq Ultrascale+ Technology
- SFP Modules for Redundant Timing and Ethernet Links



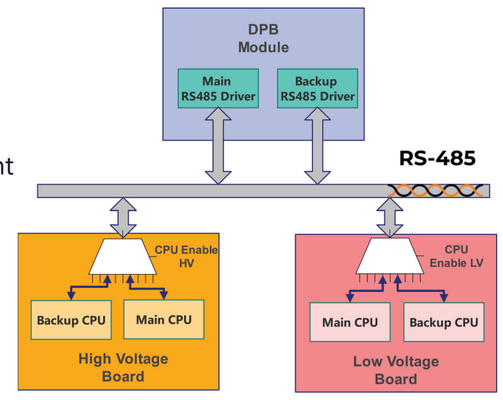
Slow Control

HV / LV control

- 2x RS485 links with redundant drivers and bus connections
- HV and LV independent CPU enable GPIOs

I2C Sensors

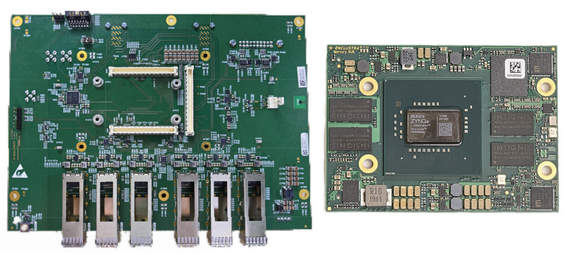
- SFP temperature, voltage and current
- On-board and in-silicon temperature



Digitizer control

- UART link for monitoring / configuration
- Per channel threshold, dead time, integration time configuration
- Temperature, Pressure and Humidity

Manufacturing



SOM + Carrier architecture

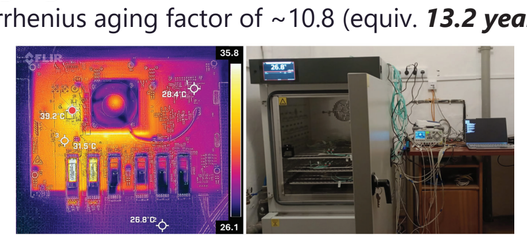
- IPC3 Compliant Manufacturing
- Flexible I/O and processing reconfigurability
- Lower Engineering costs, requiring to design only one of the two parts of the design
- Simplicity in the routing of the carrier by moving the complex components to the SOM
- ***Design proved in three prototypes across 3 years***

Reliability

Predictions

FIT Figure of 1352, corresponding to a Mean Time Between Failures of 740,000 hours

- **Reliability optimized**, using SN29500 and HDBK-217Plus:2015
- **Mix of Automotive and Industrial grade components** for best expected reliability at reasonable costs
- **Aging test**: 3 units, no failures, 15 months@60ºC Arrhenius aging factor of ~10.8 (equiv. ***13.2 years***)



Hardware Implementation

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