MicroTCA-based low latency data streaming and processing architecture using UDP offload and Time Sensitive Networking

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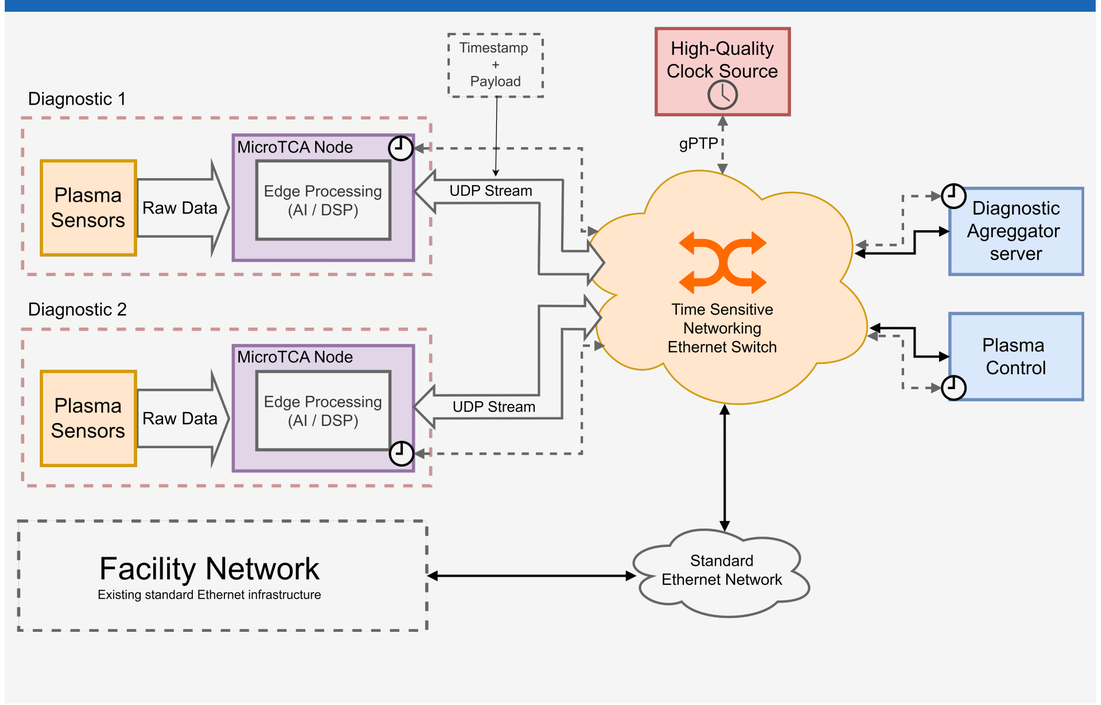
Abstract

As experimental fusion devices transition from shot-based operation to longer pulse duration, diagnostic and control systems need to evolve to support this kind of operation. This work proposes a distributed data acquisition architecture that aims to provide ultra-low latency communications based on full hardware User Datagram Protocol (UDP) offloading, leveraging the emerging IEEE Time Sensitive Networking (TSN) technologies for deterministic latency and synchronization, and providing an edge computing platform that allows the implementation of Digital Signal Processing (DSP) algorithms and Artificial Intelligence (AI) real-time using High-Level Synthesis (HLS). The solution proposes the use of the Micro Telecommunications Computing Architecture (MTCA) standard as the foundation and is entirely built from Commercial Off-The-Shelf (COTS) components.

System Architecture



Acknowledgements

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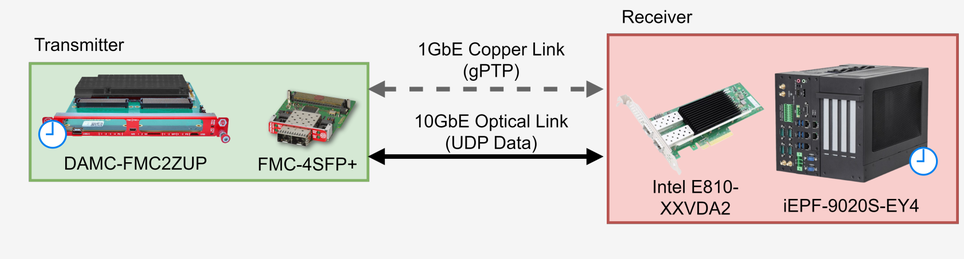
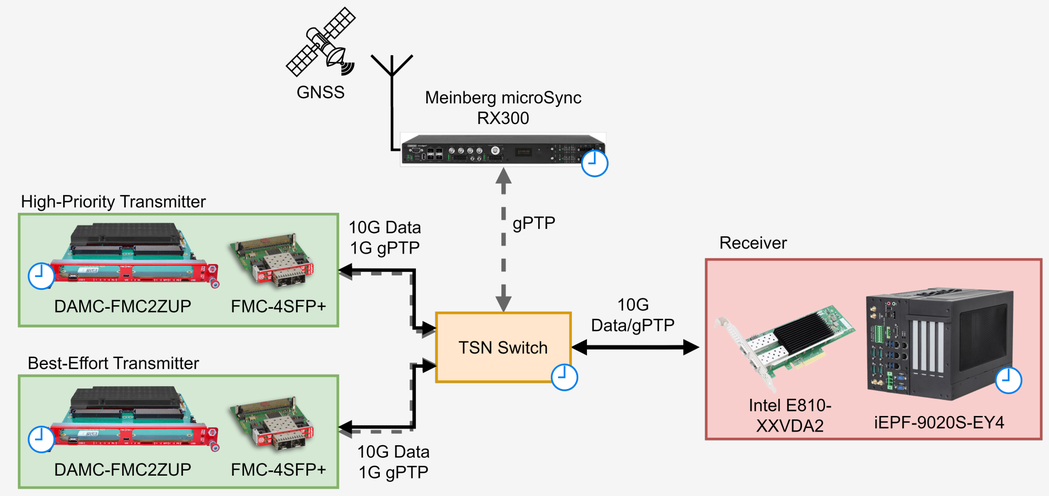
Experimental Setups



(a) Point-to-Point Setup



(b) Complete Setup

Implementation

DAMC-FMC2ZUP

FMC-4SFP+

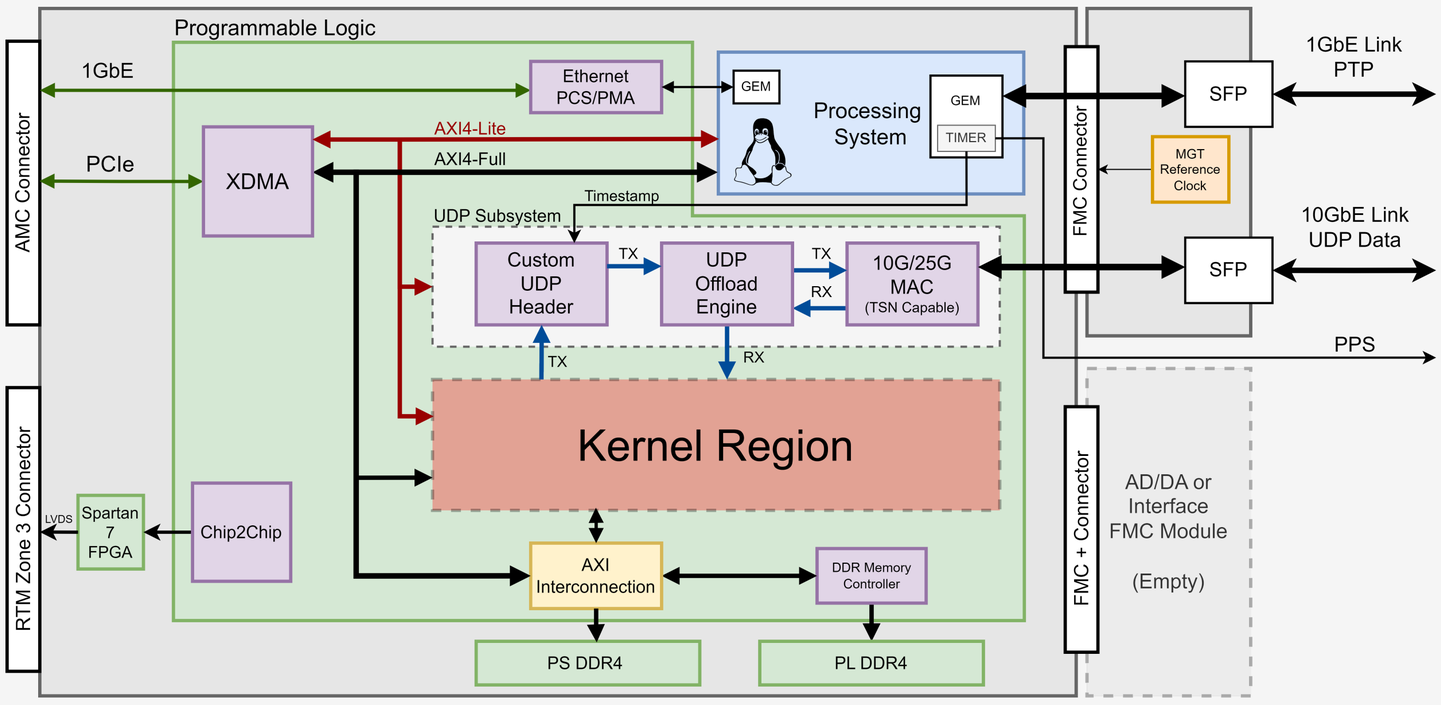


Figure: Zynq UltraScale+ MPSoC hardware block diagram for DAMC-FMC2ZUP

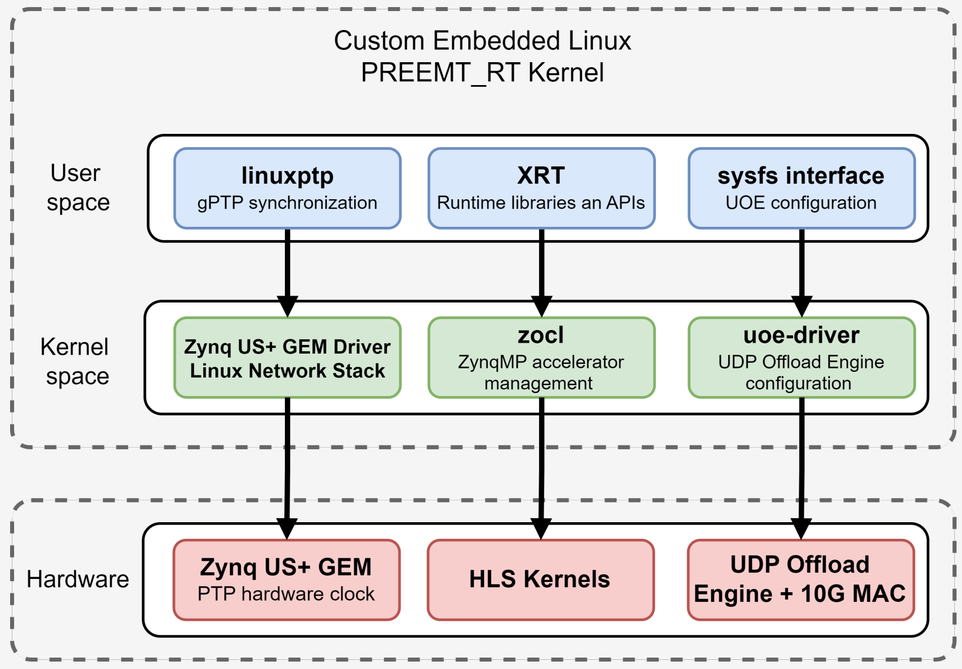
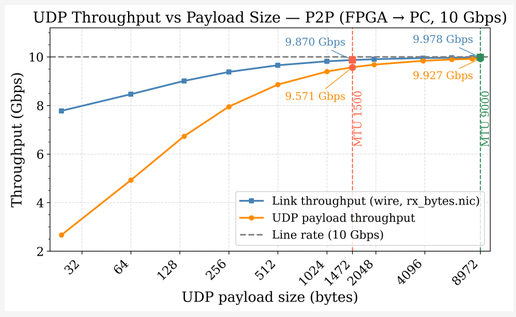
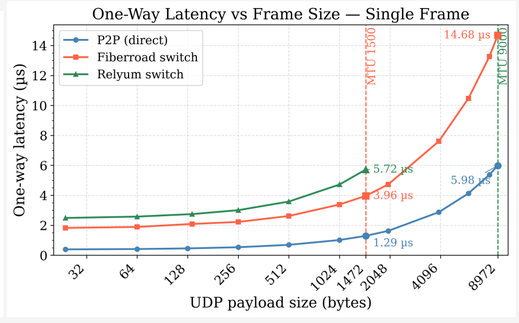


Figure: Embedded Linux software stack

Results





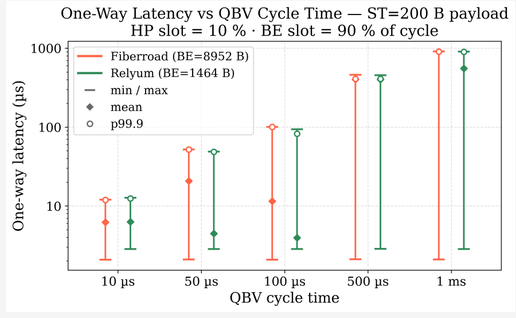


Table: FPGA Resource Utilization

Resource	Used	Available	Used (%)
LUT	89,183	522,720	17.06
LUTRAM	14,055	161,280	8.71
FF	125,782	1,045,440	12.03
BRAM	98	984	9.96
DSP	3	1,968	0.15
PLL	1	22	4.55

Table: gPTP synchronization performance.

Setup	Link	Mean (ns) Corrected	Mean (ns) Uncorrected	Std (ns)	Max (ns)	Min (ns)
S1	GM→Node	0.149	-213.09	4.237	15	-20
S3 (FR)	GM→SW	-	-	-	-	-
	GM→Node	0.55	-211.74	4.78	15.5	-16.5
S3 (RE)	GM→SW	-1.193	-1.193	27.307	91	-81.5
	GM→Node	0.041	95.819	21.947	64.5	-56

FR: Fiberroad FR-TSN4412, RE: SoC-e RELY-TSN12

Conclusions

- Validated MicroTCA-based distributed data acquisition architecture, enabling real-time diagnostics correlation
- HLS-based DSP and AI algorithm deployment with partial reconfiguration support
- Near wire-speed UDP offload: 9.927 Gbps application-level throughput with low end-to-end latency and jitter
- gPTP synchronization with sub-5 ns standard deviation, enabling precise timestamping across distributed acquisition nodes
- TSN Time-Aware Shaper provides strict bounded latency for mixed-criticality traffic, with guarantees down to 10 µs cycle times