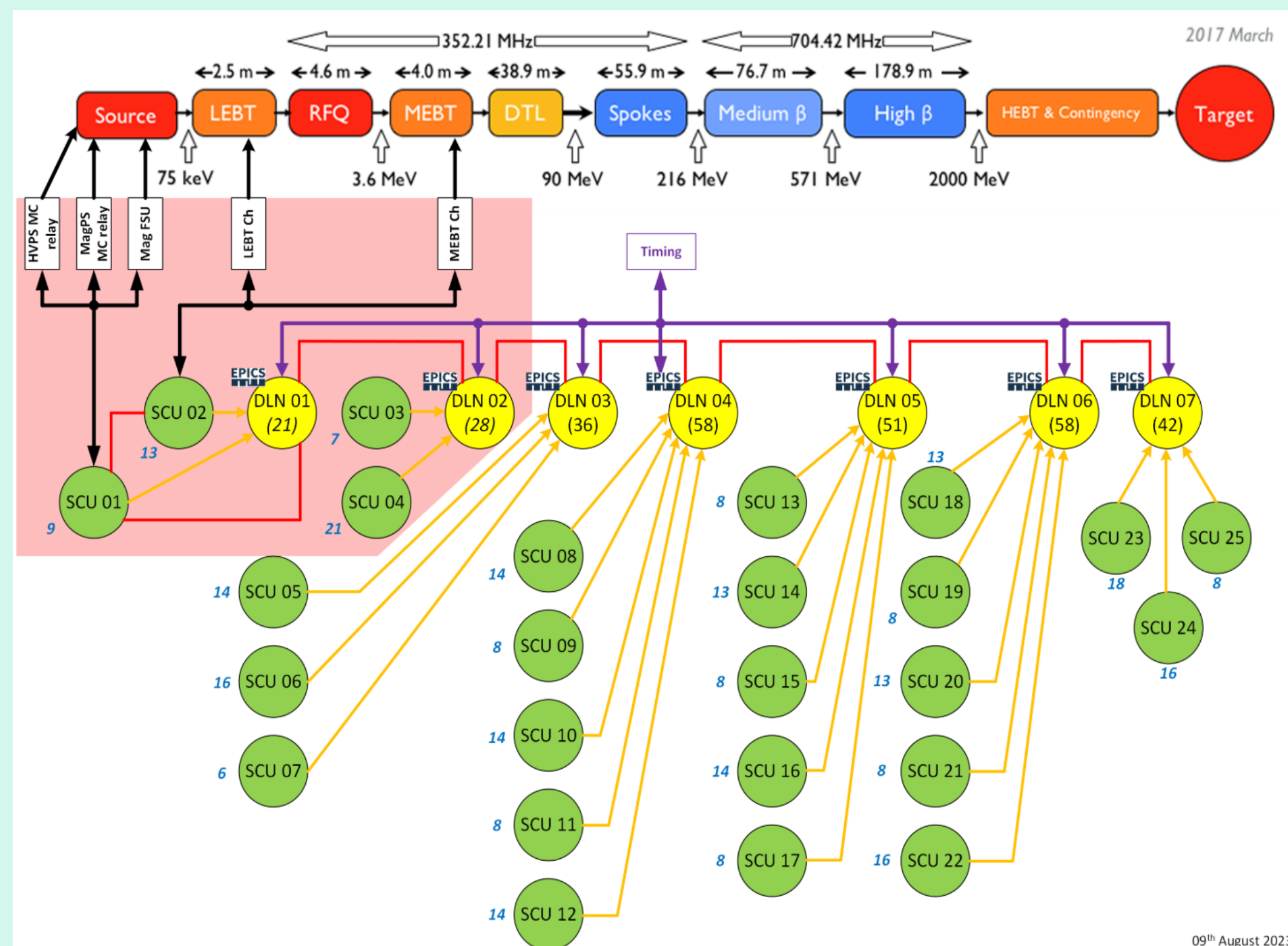


# Modular Hardware, Firmware, and Control-System Integration: Lessons from Commissioning the Fast Beam Interlock System at ESS

S. Pavinato, A. Nordt, E. D'Costa, M. Carroll, R. Xavier da Silveira, S. Gabourin  
European Spallation Source, Lund, Sweden

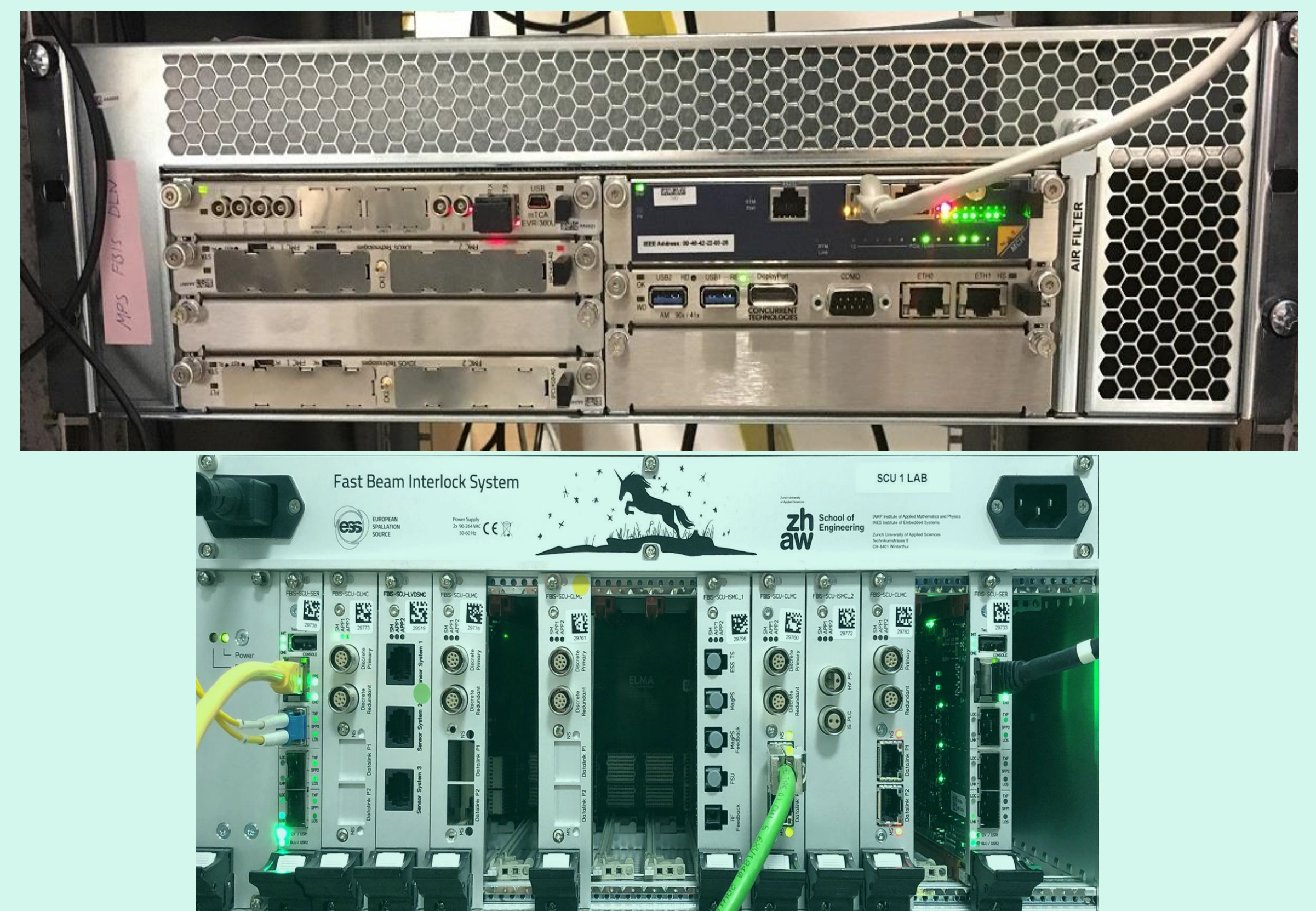
The Fast Beam Interlock System (FBIS) at the European Spallation Source (ESS) is a distributed, safety-critical system that collects status information from multiple accelerator subsystems and, when unsafe conditions arise, stops both the machine and the proton beam within microseconds. During the ESS commissioning process, from integration testing to full beam operation, FBIS was developed using a modular approach for hardware, firmware, and control system interfaces. Standardized mTCA crates and cPCI platforms enabled the sharing and reuse of hardware components across different interlocking and diagnostic systems, simplifying development and maintenance. Each parameterized firmware release is validated with rigorous laboratory testing that mirrors simulation methodologies, ensuring reliable system performance before deployment and efficient management of diagnostic data and events during operations. System timing ensures precise alignment of diagnostic data across FBIS crates. This paper summarizes the practical and architectural lessons learned from the implementation of FBIS, highlighting how the modular design of hardware and firmware enabled flexible adaptation, reliable operation, and a modular control system level during machine commissioning.

## System Overview



- ESS, Lund: most powerful pulsed neutron source under construction. Proton beam can damage equipment in **tens of microseconds**— the FBIS is the only system that stops beam and machine in time.
- 600 m linac, ~250 sensor systems connected (mostly FPGA-based)
  - 32 crates: 7 mTCA DLNs (Kintex Ultrascale) + 25 cPCI SCUs (Zynq Ultrascale+ MPSoC)
  - Fully redundant. FBIS meets **Protection Integrity Level 2**
  - SCU → DLN via Aurora 64b/66b optical Slink + OPL for Global Beam Permit
  - Synchronization via MRF timing system (GPS PPS → EVR → mLVDS backplane)

## Modular Hardware



- Standardized** mTCA and cPCI platforms enable hardware reuse across FBIS and the wider ESS ecosystem (>300 mTCA systems across RF, BI, MP, TD).
- FAT testers built on the **same mTCA crates** as the operational DLN
  - Bitstreams deployed via Ansible playbooks / GitLab CI. Fully remote, reproducible and trackable.
  - PROFINET interface (PLCs ↔ FBIS): host application written entirely in VHDL, mirroring Anybus CompactCom state machine over SPI at 20 MHz
  - ESS FPGA Framework: AXI4-based common platform for mTCA FPGA developments; future target for DLN register interface migration from TOSCA

## History Buffer

- Every FPGA contains a firmware History Buffer (HB): nanosecond-resolution rolling record of state transitions.
- 1024 records per node; 128-bit records (timestamp, system ID, event type, details)
  - Simultaneous trigger snapshot mechanism prevents timestamp skew between concurrent events
  - GPS PPS synchronization across all DLN HBs → super HB: full cross-crate event timeline within 14 μs

## Firmware Verification

- Unified Python framework closes the gap between simulation and hardware testing. Hence same codebase, same scenarios, same reports.
- **Cocotb** (simulation) + **Pytest** (FAT hardware) : same parametrized test scenarios, JUnit XML output, GitLab CI/CD
  - UVM-inspired: shared Environment / Driver / Monitor / Scoreboard. Scoreboard reused unchanged across sim and hardware. RTM traceability: SRS → DDS → test; both simulation and hardware must pass each requirement

## Takeaways

- **Modular hardware** + ESS FPGA Framework (AXI4 + XDMA): same boards, same PCIe driver across nodes and systems. Engineers focus on custom logic design and testing, not on device support
- Modular mTCA hardware. FAT testers reuse operational boards : faster and more trusted FAT
- **Unified Python framework**: same scenarios drive simulation and hardware validation
- JUnit XML + RTM across sim and hardware : straightforward audit and traceability
- Next: full super-HB across SCUs + automated root cause analysis tool