

Synchronization of PLC Subsystems with the Timing Distribution System at the European XFEL

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Abstract—The European XFEL generates bursts of up to 4096 ultra-short X-ray flashes with a spacing of only 222 ns every 100 ms. These flashes are produced in the linear electron accelerator by undulators and guided 1 kilometer in vacuum pipes until they reach the scientific experiments. Accurate synchronization and the availability of information about all configurable pulses within a single burst, which can vary every 10 Hz cycle, enable the full potential of control, monitoring, and measurement in terms of accuracy and utilization. The MicroTCA-based timing system provides all the necessary capabilities. However, the industrial programmable logic controllers (PLCs), which manage most of the control electronics of the beamlines and experiments, are only synchronized on a millisecond-level through UART and NTP interfaces. This paper presents a new development based on an FPGA SoC EtherCAT solution in MicroTCA that implements an interface to the PLC using distributed clocks to achieve synchronization on nanosecond-level and provide beam-related information in a deterministic manner.

Index Terms—EtherCAT, timing system, synchronization, PLC

I. INTRODUCTION

THE European X-Ray Free-Electron Laser (XFEL) is a research facility in Schenefeld, Germany, that provides high-brilliance X-ray beams to seven scientific instruments [1]. A 3 km long superconducting linear accelerator, originating at DESY (Deutsches Elektronen-Synchrotron) in Hamburg, accelerates electrons to 17.5 GeV and delivers the beam to three beamlines at the facility, where the undulators use the self-amplifying spontaneous emission effect [2] to generate coherent X-ray light from the electrons. Figure 1 shows the pulse structure of the beam. The accelerator delivers beam in a 900 μ s train within a 100 ms accelerator cycle. A train can contain up to 4096 pulses, each with a duration of less than 25 fs, while adjacent pulses are separated by 222 ns. The instruments use the resulting X-ray light with wavelengths between 0.50 Å and 47 Å and ultra-short pulse duration to study the dynamics of chemical reactions in organic and inorganic samples, as well as fundamental light-matter interactions.

The beamlines in the facility and the instruments use industrial automation solutions based on the Programmable Logic Controllers (PLCs) and bus terminals. Until now, we have configured and operated these solutions synchronized via the Network Time Protocol (NTP) which is far too imprecise for scheduling events relative to the arrival time of X-ray pulses.

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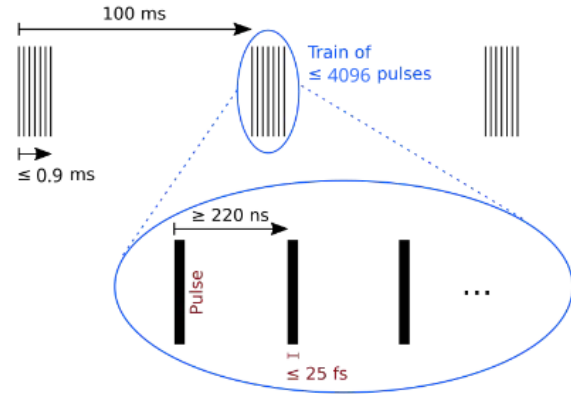


Fig. 1. Pulse structure of the beam at the European XFEL

This paper describes the synchronization of the PLC system with the facility timing distribution system with nanosecond-level precision using the Distributed Clocks (DC) [3] mechanism of the EtherCAT fieldbus, thereby enabling hardware control based on beam timing and bunch energy. Better synchronization opens opportunities to improve system control and enable more sophisticated measurements with the PLC system.

The paper has the following structure: section II describes the PLC subsystem and the EtherCAT fieldbus, section III gives the overview of the timing information distribution system at the European XFEL, section IV describes the hardware board and the FPGA-based synchronization mechanism, section V describes the test setup and measurement of system synchronization, and section VI gives an outlook for possible applications of the system at the European XFEL.

II. PLC SYSTEM AT THE EUROPEAN XFEL

There are more than 7000 PLC terminals at the European XFEL. We use the PLC system to control electro-mechanical components of the scientific instruments, measure their position, control and monitor vacuum components, and in safety applications to protect the equipment.

To simplify maintenance and speed up development cycles, the PLC team at the European XFEL decided very early on to use the PLC terminals and software from Beckhoff GmbH exclusively [4]. The Beckhoff PLC software and terminals natively use EtherCAT [5] fieldbus for communication.

EtherCAT is a real-time Ethernet communication protocol based on the 100Base-TX Ethernet standard [6] and later re-

vised to support faster Ethernet standards. The fieldbus always requires a master device, which initiates the transaction. This is usually a software running on an industrial PC. All slave devices are connected in a loop, a star, or a mixed topology. In the loop topology, the devices are connected in the daisy chain and EtherCAT frames traverse all devices, exchanging data on the fly as they pass through each device. In the star topology, the devices are connected directly to the master. The mixed topology is the mixture of the star and the loop topologies.

The distinctive feature of EtherCAT, the Distributed Clocks, is its deterministic transport latency and drift compensation which corrects differences in clock frequencies between endpoints. The DC makes it possible for the PLC software to synchronize system time counters in the terminals with a precision below 100 ns [3]. All terminals in the loop get a common time reference frame and, therefore, can reliably exchange the timestamp of events from different devices in the same loop.

EtherCAT implementations follow the OSI model [7]. The physical layer is implemented in Ethernet PHY ASICs supporting 100Base-TX. The data link layer requires real-time data processing and is implemented in an ASIC or an FPGA. The application layer can be implemented in software or in firmware. In this work, we implemented both the data-link and the application layer in FPGA firmware.

III. TIMING DISTRIBUTION SYSTEM

The timing distribution system is a hierarchical system used for control of the electron accelerator [8]. The timing system distributes accelerator clock and beam configuration through the network of timing boards to detectors and data acquisition hardware.

The timing distribution system of the facility is based on the x2timer [9] boards in the Advanced Mezzanine Card (AMC) form-factor. The boards build a multi-level timing distribution system using 1.3 Gbps serial optical links with drift and offset compensation to distribute beam information. The boards provide the following information about the accelerator cycle:

- the unique cycle ID (train ID),
- the precise timing for the start of the accelerator cycle,
- the full table of pulses, and
- the beam mode, which provides the mask of the active segments in the accelerator.

The pulse table can change from cycle to cycle and consists of entries containing pulse information: pulse position, pulse charge, and destination beamline. The final-level timing board decodes this information and provides it over a 108 Mbps Universal Synchronous and Asynchronous Receiver-Transmitter link, USART, on the backplane of the Micro Telecommunications Computing Architecture (uTCA) crate to other boards for synchronization.

In addition, the timing system provide a reduced subset of the timing information over a 115 kbps USART link to the PLC system. The reduced subset of the timing information includes only the train ID and the beam mode. Receiving this information signals the start of a new accelerator cycle to the PLC system which can use this as a trigger for its actions.



Fig. 2. The Zynq UltraScale+ MPSoC board in the uTCA form factor we use for interfacing the timing distribution system to the PLC system over EtherCAT interface.

The low data rate limits the amount and timing precision of information and makes synchronous operation of the PLC system with the accelerator impractical for fast control. At the moment, changing or measuring the position of the mechanical equipment requires disruption to data acquisition as we have large uncertainty about the read-out time relative to the arrival time of X-ray pulses. The following section presents our approach to bridge the timing distribution and the PLC systems, and make precise information about the beam and its timing available to the PLC terminals.

IV. PLC SYNCHRONIZATION WITH THE TIMING DISTRIBUTION SYSTEM

A. Synchronization Principles

The PLC and the timing systems use two independent time reference frames. Therefore, we must find a common reference frame for both systems or convert the time between the reference frames. Because the timing metadata carries an NTP timestamp of the start of cycle pulse, we evaluated passing this timestamp to the PLC system, but decided against it because NTP does not provide sufficient precision.

We decided to use the backplane trigger signal which is generated by the x2timer instead. The x2timer generates this signal with picosecond precision and the FPGA measures its arrival time in the reference frame of the EtherCAT distributed clocks in the clock domain of the 100 MHz EtherCAT clock. Thus, the resulting timestamp has a precision of 10 ns and, because the time counters in the endpoints are synchronized via the DC mechanism, the timestamp maintains a fixed relation to the beam and can be used to calculate all further actions.

B. Hardware

At the European XFEL, we maintain uTCA-based infrastructure consisting of timing distribution systems and analog-digital converter boards. Therefore, we require the bridge hardware to be in the uTCA form factor. Further requirements in-

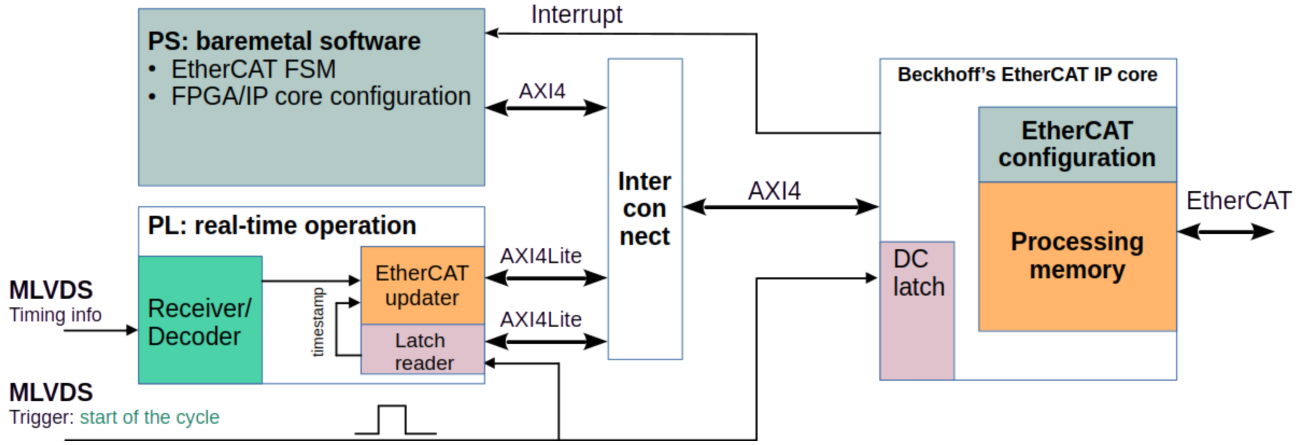


Fig. 3. Layout of the firmware for the communication bridge. The firmware consists of the Beckhoff IP core for EtherCAT communication, baremetal software in the processing system for non-real-time control, and the real-time data processing in the programmable logic.

clude EtherCAT-compatible network interfaces, and an FPGA-based processing system for real-time data processing and communication.

As there were no boards on the market that satisfied our requirements, we collaborated with the N.A.T. GmbH to produce a board in the uTCA form factor with the capabilities listed above. Figure 2 shows the picture of the produced NAT-AMC-ZYNQUP-ECAT board [10].

The board is built around the Zynq ZynqUltraScale+ Multi-processor System-on-Chip (MPSoC) XCZU2CG. The MPSoC is connected to the backplane on the AMC connector, from where it receives timing metadata and the precise start-of-cycle pulse from the x2timer over the Multipoint Low-Voltage Differential Signaling (M-LVDS) lines, and to 8 RJ45 ports on the front panel, each capable of 100 Mbps Ethernet communication.

To attach a board to the EtherCAT loop, we need a minimum of two RJ45 ports. Therefore, the board can be used to supply timing information to 4 PLC loops in parallel.

C. Firmware

Figure 3 shows the layout of the firmware designed for the communication bridge. The firmware consists of the EtherCAT IP core [11] for communication with EtherCAT endpoints, real-time data processing block in the programmable logic, and the baremetal software for non-realtime configuration in the processing system of the MPSoC.

To communicate with EtherCAT endpoints, the device must implement an EtherCAT slave controller in the data link layer and an application layer. A typical EtherCAT terminal usually uses an ASIC as an EtherCAT slave controller. In this paper, we use the EtherCAT IP core v3.00k from Beckhoff to implement the EtherCAT slave controller. The IP core takes over the steering of the Ethernet PHY chips, EtherCAT communication, and synchronization and drift compensation for the distributed clocks.

For data exchange with the data processing logic, the IP core provides memory-based access through the Advanced eXtensible Interface 4 (AXI4) interface. The memory is subdivided

into two regions: the EtherCAT **configuration** memory and the **processing** memory. The EtherCAT configuration memory is the unbuffered memory accessible to both the PLC master and the processing logic. It contains the registers common to all EtherCAT slave controllers that are necessary for communication over the fieldbus. The configuration memory plays an essential role in establishing communication and identification of the device. The processing memory is a memory available for exchanging information between the PLC master and the application layer on the device.

As an additional feature, the IP core provides a distributed clock latch function which latches the timestamp of the rising edge of the received signal and stores it in the EtherCAT configuration memory.

The baremetal software configures the on-board hardware, monitors and reacts to the interrupts from the IP core to configure the device ID and establish the EtherCAT communication. After communication is established, the software is responsible for changing the states of the EtherCAT finite-state machine in response to the PLC master request, and acknowledging the state transition.

The application layer in the programmable logic receives timing metadata from the x2timer and decodes them. The logic also implements two AXI4Lite master modules. One master reads the timestamp from the EtherCAT configuration memory. Another master reads the timing metadata and the timestamp, and writes them to the processing memory of the IP core. When the last memory address in the IP core is accessed, the IP core marks the buffer as finished, and the written information is available to be accessed by the PLC master.

The AXI4Lite master that writes data to the processing memory and the PLC master must use synchronized mapping of the information stored in the processing memory. Unsynchronized mapping can lead to delays in accessing data by the PLC rendering the data out of date or causing data misalignment. To avoid this situation, we define memory content in a SystemRDL [12] file and use this file to generate the AXI4Lite master and the EtherCAT SubDevice Information (ESI) XML



Fig. 4. uTCA crate with the timing system (second board in the right column) and the EtherCAT bridge (top board in the left column).

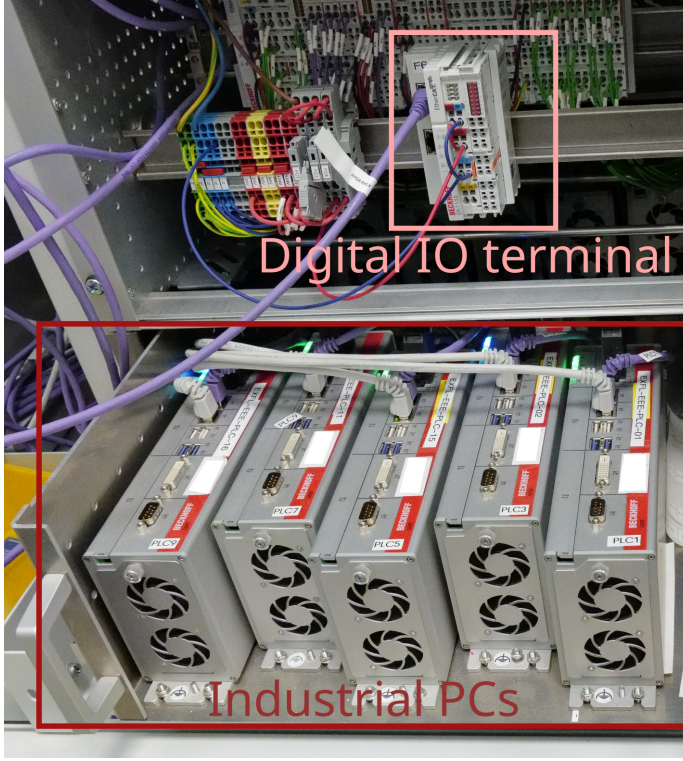


Fig. 5. PLC subsystem: industrial PCs (below) and the digital IO terminal EL2258 (upper right).

file for the PLC software. To use the PeakRDL framework [13] for the generation of the master module and the XML file, we designed the PeakRDL plugins and offer them as open-source software [14], [15].

V. MEASUREMENT OF SYNCHRONIZATION ON A TEST STAND

To test the synchronization between both systems, we built a test setup consisting of a uTCA crate and the PLC components. Figure 4 shows the uTCA crate. The crate contains the x2timer board in the second slot of the right column, which receives timing metadata from another x2timer over a yellow optical fiber. The x2timer distributes the timing metadata over the backplane of the uTCA crate to other boards in the crate. The EtherCAT bridge board is installed in the uppermost slot in the left column. Two ports of the board are connected to the PLC master and to the digital IO terminal EL2258 [16] shown in the figure 5. The PLC master software is running on an industrial PC under the Windows operating system. Multiple industrial PCs are visible in the low part of the photo. The

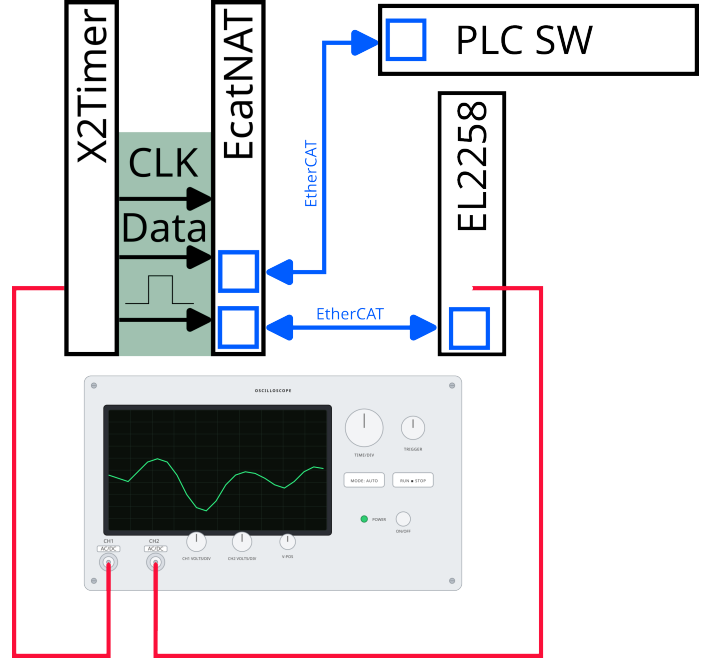


Fig. 6. Layout of the setup for testing the synchronization between the timing distribution and the PLC systems.

EL2258 terminal is visible in the upper right corner of the photo.

Figure 6 shows the layout of the test setup. The x2timer generates timing metadata and the start-of-cycle pulse, and distributes them to the EtherCAT bridge board over the uTCA backplane. In addition, the x2timer also provides the start-of-cycle pulse to the input of the oscilloscope LeCroy WR640ZI [17]. The EtherCAT bridge board latches the arrival time of the start-of-cycle pulse, and makes its timestamp available for the PLC master to read over EtherCAT. The PLC master software reads the timestamp from the EtherCAT bridge board, adds a constant delay of 6 ms, and programs the digital IO terminal to generate a pulse precisely 6 ms after the start-of-cycle signal. The digital IO terminal provides the output signal to the oscilloscope which measures the time difference between the start-of-cycle signal and the output of the digital IO terminal.

Figure 7 shows the distribution measured by the oscilloscope. The peak-to-peak spread of the distribution is $49.8\mu\text{s}$ and the full width at half maximum (FWHM) is $20\mu\text{s}$. The measurement is consistent with the execution time of the EL2258 terminal of less than $40\mu\text{s}$ [16].

To eliminate the measurement limitation due to the precision of the signal generation in the terminal, we replaced the terminal with the second EtherCAT bridge board and kept the PLC software algorithm the same. Figure 8 shows the layout of the updated setup. Since the EtherCAT bridge board lacks digital outputs from the FPGA, we sent the generated pulse to a SIS8300-KU board over the uTCA backplane. The FPGA in the SIS8300-KU board asynchronously forwards the signal from the backplane to the front panel digital output, which we connect to the oscilloscope to measure the time difference between the pulses.

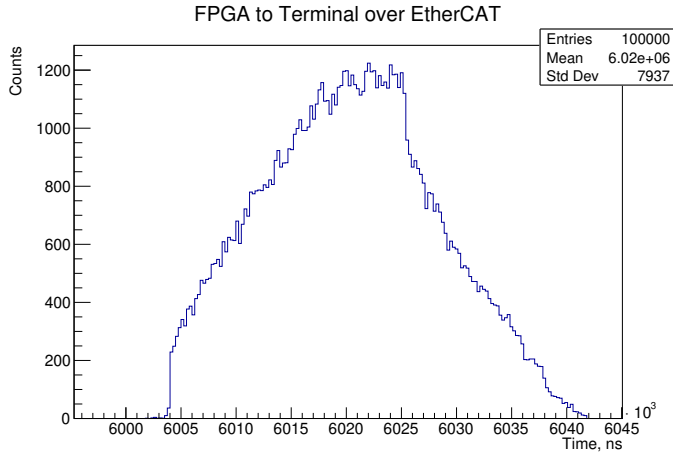


Fig. 7. Measured time difference distribution between the trigger signal from the timing system and the pulse generated by the digital IO terminal.

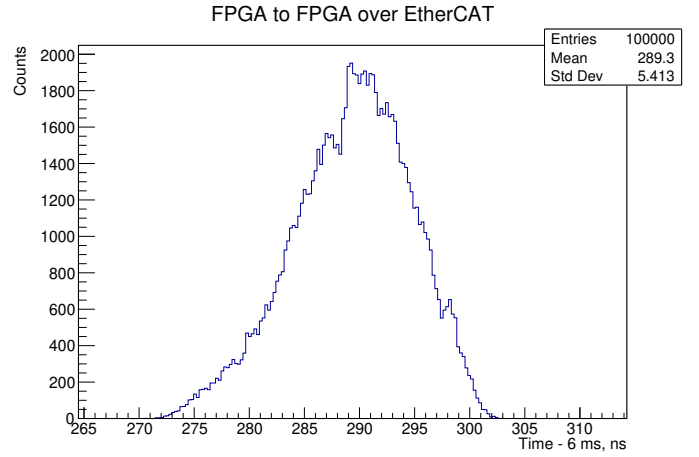


Fig. 9. Measured time difference distribution between the trigger signal from the timing system and the pulse generated by the second EtherCAT board, unconnected to the timing system.

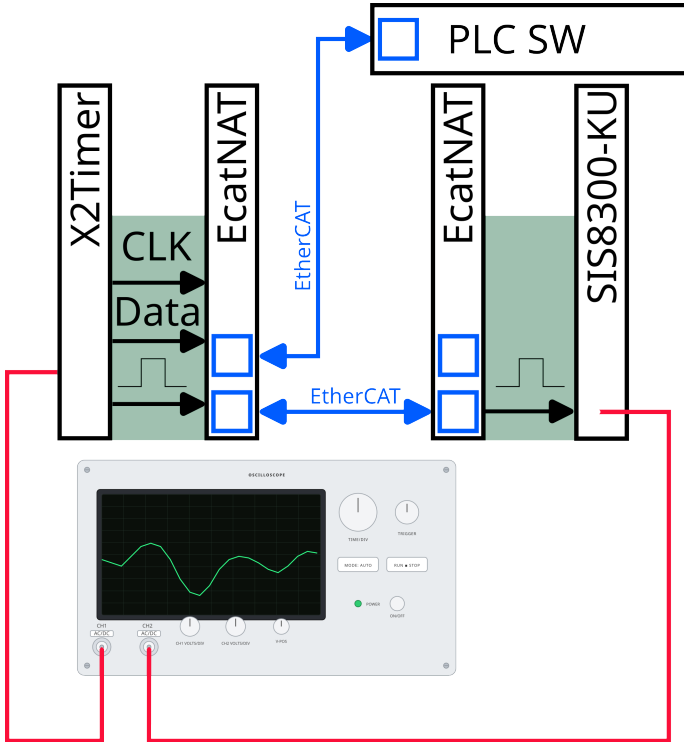


Fig. 8. Layout of the setup for testing the synchronization between 2 EtherCAT bridge boards over EtherCAT.

Figure 9 shows the distribution acquired with two EtherCAT bridge boards communicating over EtherCAT. The peak-to-peak spread of the distribution is 49.8 ns and the FWHM is 12.8 ns. This result confirms that the distributed clocks mechanism of the EtherCAT fieldbus can maintain synchronization between endpoints within 50 ns. This result is also important because the terminals use a dedicated ASIC to implement EtherCAT slave controllers, whose precision should be compatible with that achieved by FPGA-based endpoints. The performance degradation which we observed in the first test can be explained by the use of a slower microcontroller in the application layer of the digital IO terminal.

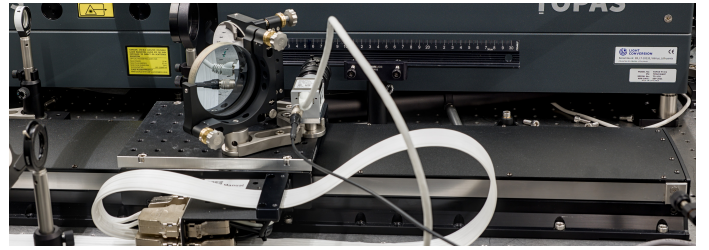


Fig. 10. The optical delay line at the FXE instrument. The retroreflector moves along the ODL changing the distance traversed by the optical laser light to change the delay between the optical and the X-ray LASERS in femtosecond range.

VI. POSSIBLE APPLICATION OF THE SYNCHRONIZATION MECHANISM AT THE FEMTOSECOND X-RAY EXPERIMENTS INSTRUMENT

The first application of the proposed solution that we identified is the synchronization of the optical delay line (ODL) with the beam at the Femtosecond X-ray Experiments instrument (FXE) [18].

Most experiments at the FXE instrument are carried out to measure the structural evolution of matter during chemical reactions or phase transitions. This is done by pump-probe measurements, where the delay between two pulses is varied: The first commonly is an optical excitation pulse that initiates a process and the second is a subsequent X-ray probe pulse that measures the atomic or electronic structure. Both pulses have durations of a few femtoseconds and therefore the delay between the pulses is commonly controlled with few femtosecond accuracy. Most of the dynamics under investigation are measured over a 100 ps delay range, which corresponds to a 7.5 mm scan range on an ODL that scales four light paths. These experiments are often conducted in a stepwise fashion where probe data are accumulated statically at several delay steps. However, to avoid drift of beam conditions and degradation of the sample during the lengthy delay scans, several user groups have explicitly requested continuous scans of the ODL to accumulate data at all relevant delay positions

effectively simultaneously. This requires moving the ODL with velocities up to 2 mm/s, so that every second a full delay scan covering 27 ps delay range is executed. Accepting a 3 fs timing jitter due to readout inaccuracies of the ODL corresponds at 2 mm/s to an acceptable readout timing jitter of 200 μ s. Specifically at European XFEL, continuously changing the delay implies that the pump-probe delay for the first and last pulse in a burst will be different. A common burst of 500 μ s will then cause a 13 fs timing difference from the first to the last pulse when moving at 2 mm/s, rendering this velocity the upper limit of reasonable motion speeds of an ODL at European XFEL. Therefore, continuous delay scans at reasonable ODL velocities of 2 mm/s require a readout timing stability of 200 μ s.

As we have shown in the previous section, the measured precision of the synchronization over EtherCAT is well within the timing stability required by the FXE instrument. To implement the solution, we will need to select the EtherCAT-based motor encoder with support for the distributed clocks feature and the possibility to schedule the measurement based on the distributed clocks timestamp.

VII. SUMMARY

We collaborated with N.A.T. GmbH to build a board in the uTCA form factor that bridges the timing distribution system of the European XFEL and the PLC system using the distributed clocks feature of the EtherCAT fieldbus. We have implemented the firmware and successfully achieved synchronization between both systems. By measuring the time difference between signals generated in both domains, we determined the time resolution of the proposed solution to be 49.8 ns peak-to-peak. We have also identified a possible application of the device at the FXE instrument which will allow us to improve measurement quality by reducing measurement time.

REFERENCES

- [1] T. Tschentscher, C. Bressler, J. Grünert, A. Madsen, A. P. Mancuso, M. Meyer *et al.*, “Photon Beam Transport and Scientific Instruments at the European XFEL,” *Applied Sciences*, vol. 7, no. 6, 2017.
- [2] A. Kondratenko and E. Saldin, “Generating of coherent radiation by a relativistic electron beam in an undulator,” *Part. Accel.*, vol. 10, pp. 207–216, 1980.
- [3] EtherCAT Standardization Committee, *EtherCAT Standard ETG.1000.4, V. 1.0.4*.
- [4] N. Coppola, J. Tolkiehn, and C. Youngman, “Control using bechhoff distributed rail systems at the european xfel,” *Proceedings of ICALEPCS2013*, 2013.
- [5] D. Jansen and H. Buttner, “Ethernet: Ethercat,” *Computing and Control Engineering*, vol. 15, pp. 16–21, 2004.
- [6] “IEEE Standards for Local and Metropolitan Area Networks: Supplement to Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications - Media Access Control (MAC) Parameters, Physical Layer, Medium Attachment Units, and Repeater for 100 Mb/s Operation, Type 100BASE-T (Clauses 21-30),” Institute of Electrical and Electronics Engineers, New York, NY, IEEE Standard IEEE Std 802.3u-1995, October 1995, amendment to ISO/IEC 8802-3: 1990.
- [7] J. Day and H. Zimmermann, “The osi reference model,” *Proceedings of the IEEE*, vol. 71, no. 12, pp. 1334–1340, 1983.
- [8] K. Rehlich, A. Aghababian, H. Kay, G. Petrosyan, L. Petrosyan, V. Petrosyan *et al.*, “The new timing system for the european xfel,” pp. –, 2013.

- [9] A. Hidvégi, P. Geßler, H. Kay, K. Rehlich, and C. Böhm, “Timing and triggering system for the European XFEL project - a double sized AMC board,” in *2012 18th IEEE-NPSS Real Time Conference*, 2012, pp. 1–3.
- [10] N.A.T. GmbH, Economic bridge between ethercat and mtca in double-width amc form factor.
- [11] Beckhoff Automation GmbH & Co. KG, *EtherCAT Slave Controller IP Core for Xilinx FPGAs Release 3.00k*.
- [12] Accellera, SystemRDL 2.0 Register Description Language.
- [13] Alex Mykyta, PeakRDL.
- [14] Dmytro Levit, PeakRDL AXI4Lite Master VHDL plugin.
- [15] —, PeakRDL EtherCAT ESI XML plugin.
- [16] Beckhoff Automation GmbH & Co. KG, *EL125x, EL2258 8 Channel Digital Input/Output Terminal with time stamp. Version: 3.2.0*.
- [17] Teledyne LeCroy Inc., *Operator's Manual HRO / WaveRunner 6 Zi Oscilloscopes*.
- [18] A. Galler, W. Gawelda, M. Biednov, C. Bomer, A. Britz, S. Brockhauser *et al.*, “Scientific instrument Femtosecond X-ray Experiments (FXE): instrumentation and baseline experimental capabilities,” *Journal of Synchrotron Radiation*, vol. 26, no. 5, pp. 1432–1447, Sep 2019.