# New Hardware for Synchronization of the PLC Subsystems with the Timing Distribution System at the European XFEL

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For the EuXFEL Fast Electronics Group

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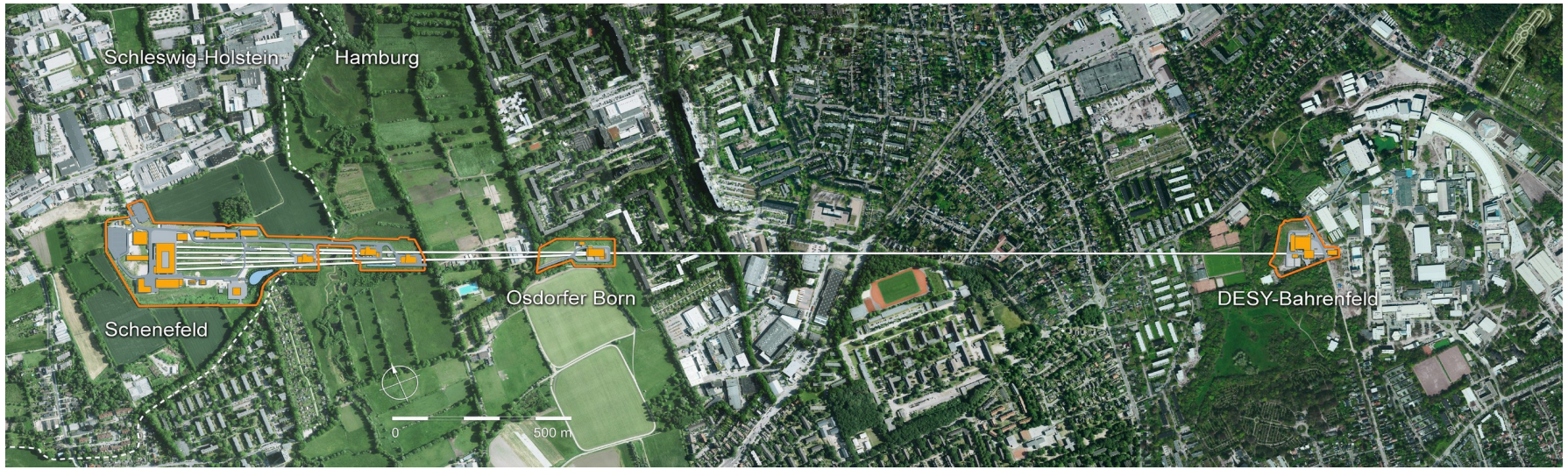
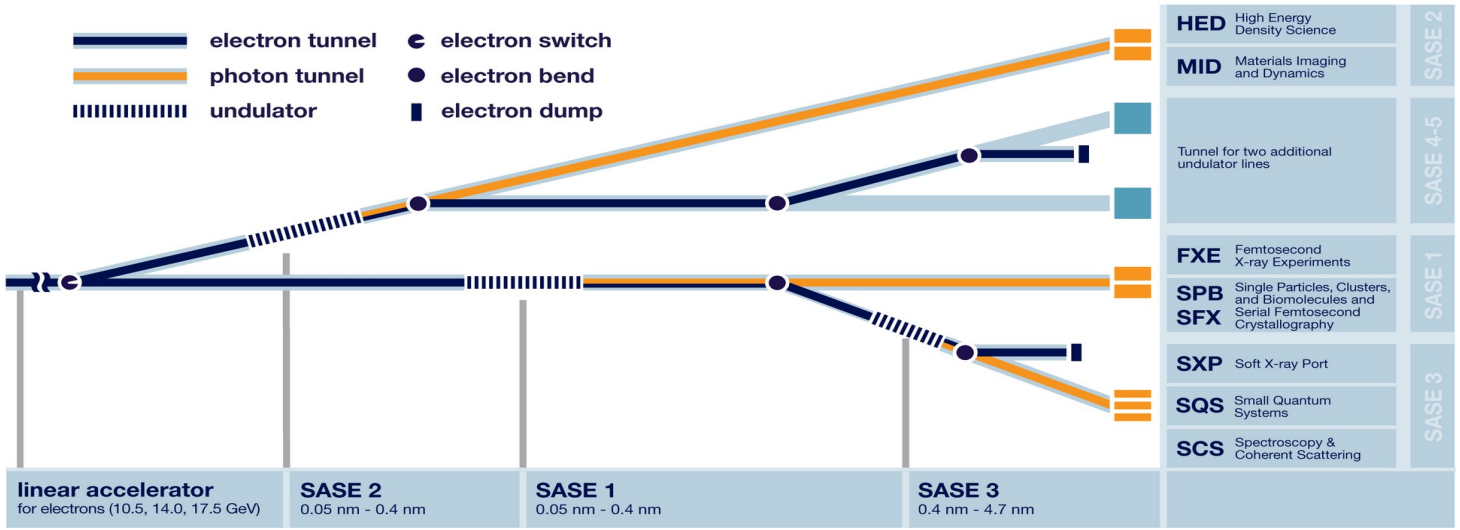
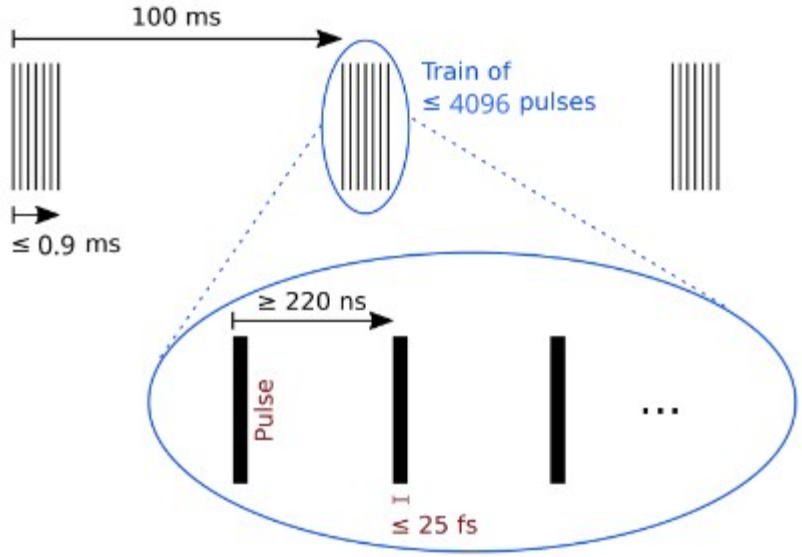
# European XFEL




- 3.4 km tunnel for beam delivery from DESY in Hamburg to Schenefeld
  - 1.7 km **superconducting linear accelerator**
  - Maximum electron energy: 17.5 GeV
-

# Timing System of the European XFEL



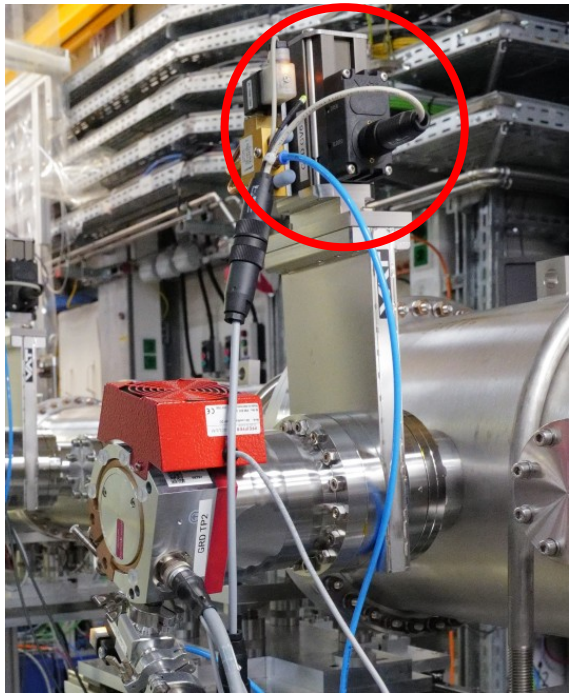



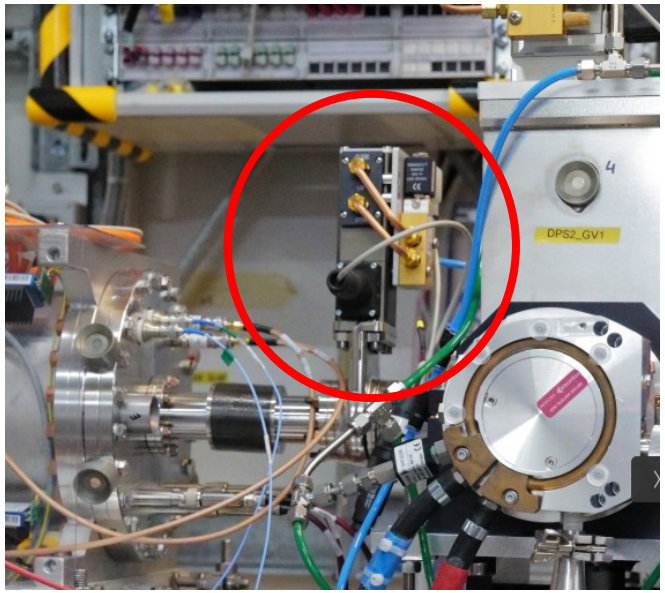

- 3 beamlines covering soft and hard photons
- 2/3 scientific instruments per beamline
- Pulses distributed among beamlines

- Trains with **10 Hz** repetition rate
- Up to **4096 pulses** per train
  - All pulses within **910 us**

# PLC System at the European XFEL

- Industrial automation within the facility
  - Motor control
  - Vacuum system control and monitoring
  - Position measurement
- Beckhoff PLC System
  - Approx 7000 terminals
- **EtherCAT** fieldbus for communication

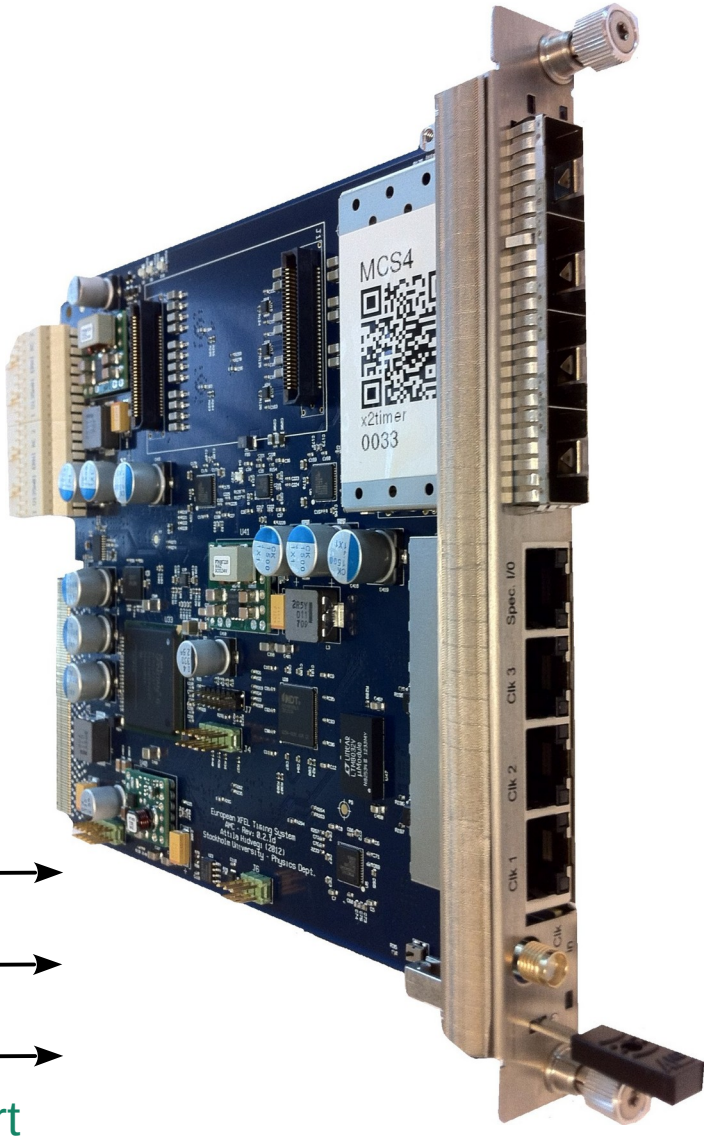


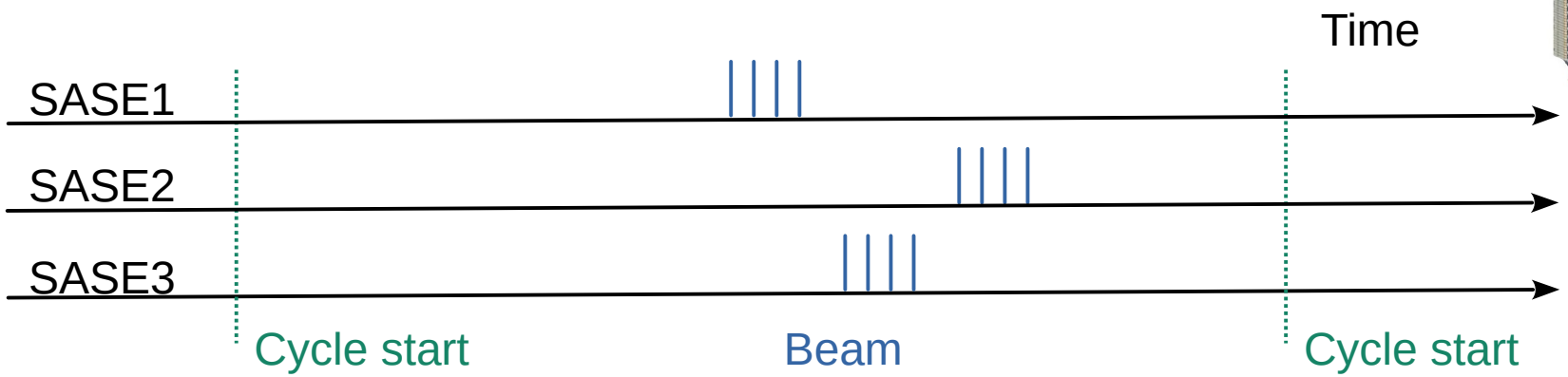



PLC-controlled motors at the SCS instrument

# Timing System at the European XFEL

- **NAT-psTimer** uTCA board for a multi-level timing distribution
  - Trigger synchronization with the jitter of 10 ps
  - **Beam bunch structure** distribution
    - Can change for each train (100 ms cycle)
  - Provides timing info on the backplane for other uTCA boards



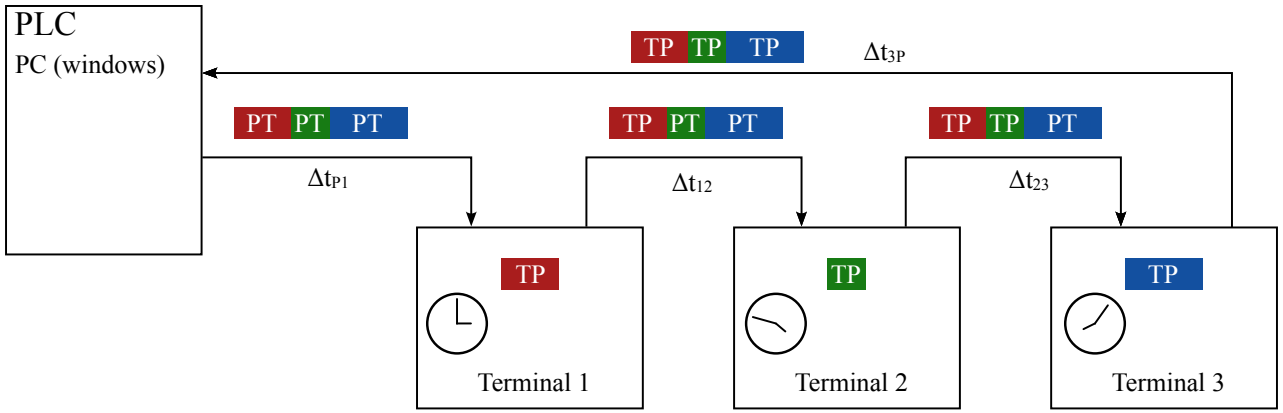



# Current Synchronization of the PLC System

- NTP synchronization with a timeserver at DESY
- UART link from timing system at **115 Kb/s**
  - **Train ID**: unique cycle identifier
  - **Beam mode**: accelerator configuration for the current cycle
- No information about
  - Precise beam timing
  - Beam structure

# EtherCAT Fieldbus

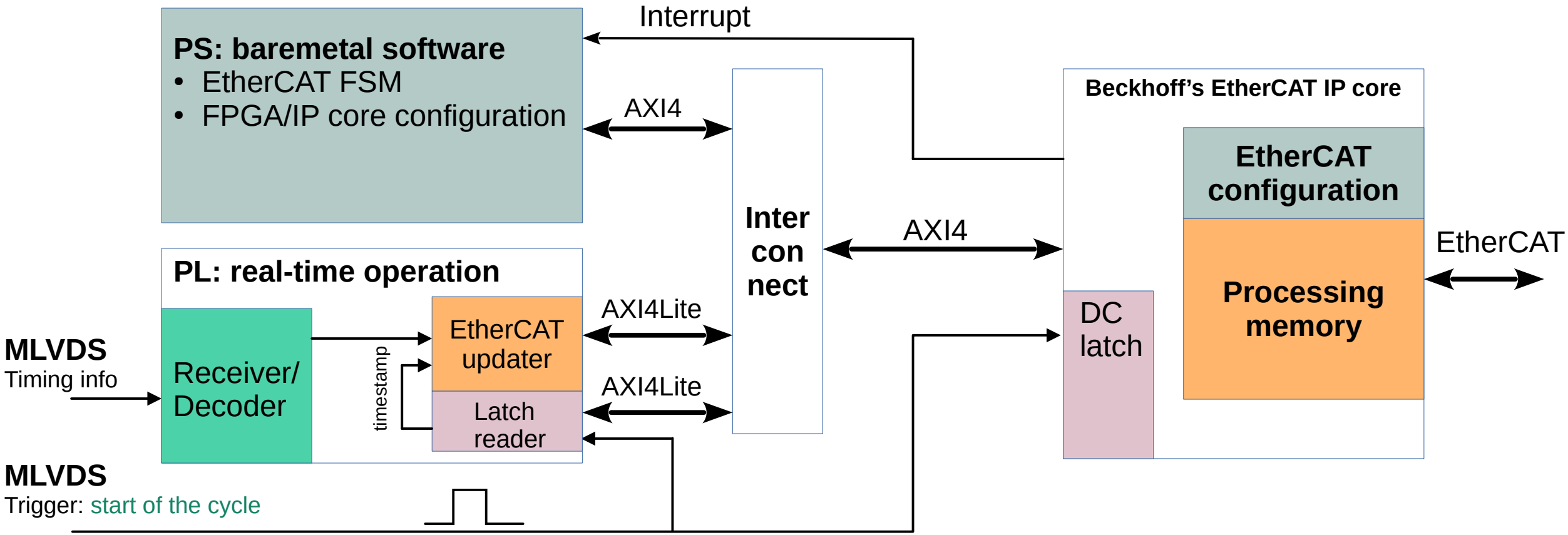
- Natively integrates with PLCs
- Based on **100BASE-TX** Ethernet standard
  - Also available for 1/10 Gb/s
- Flexible network topology
  - Linear, tree, star topologies
- Synchronization of devices in the chain
  - **Distributed clocks**
    - **Precision O(10ns)**



# Hardware Board

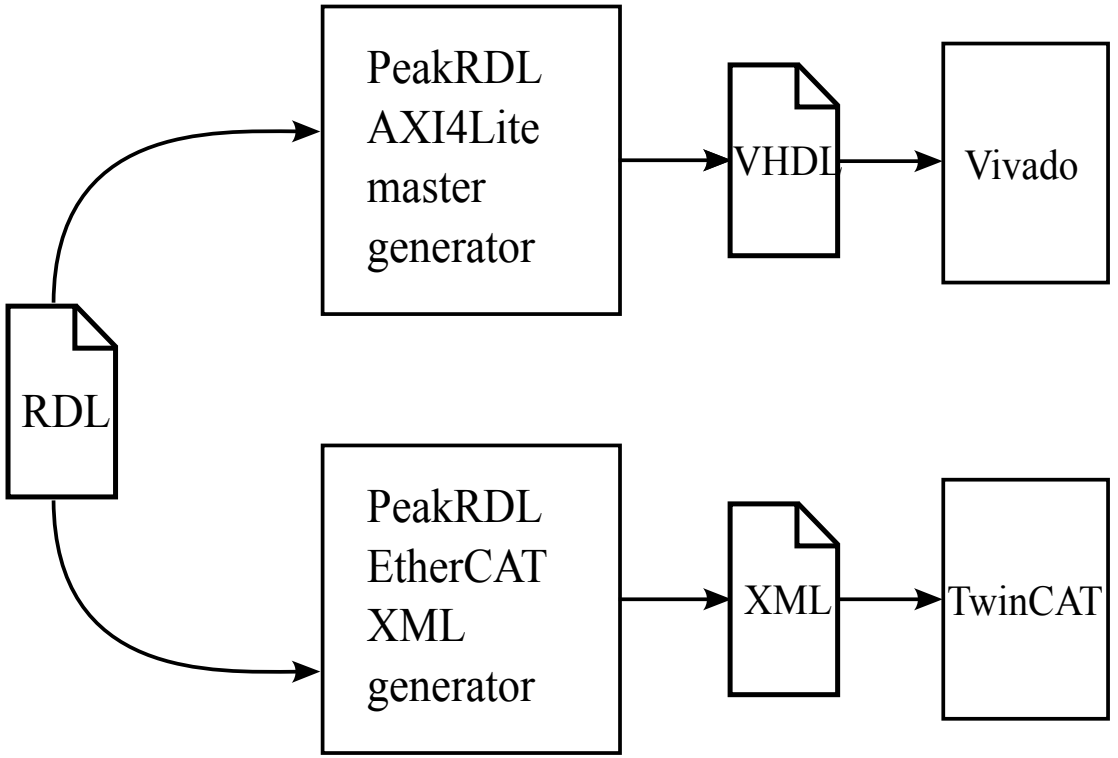
- NAT-AMC-ZYNQUP-ECAT board
  - Designed by N.A.T. GmbH using our requirements
- Board hardware:
  - uTCA form factor
  - ZynqUS+ MPSoC
  - 8 RJ45 ports
    - Possible to connect 4 independent loops
  - 4GB DDR4 RAM
  - PCIe and Ethernet on the AMC connector

# Firmware Implementation

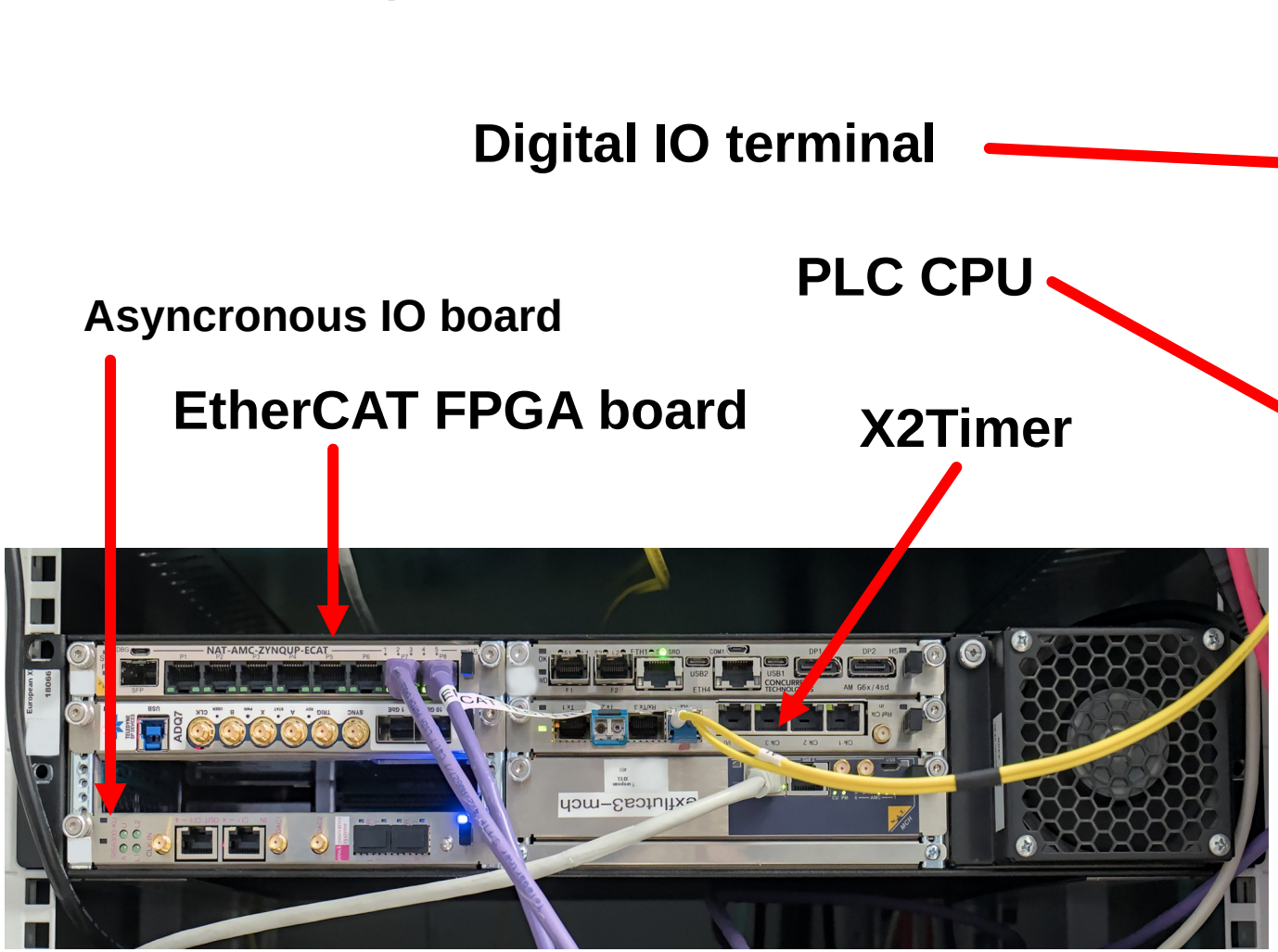


# Register Map Synchronization between FPGA and PLC

- **Single point of truth**
  - SystemRDL file
- VHDL AXI4Lite master generator from the RDL file
  - Registers → record fields
  - https://github.com/DmytroLevit/peakrdl-axil-master-vhdl
- EtherCAT slave register description for PLC software in XML format
  - **No addresses**: field position defines address
    - Empty fields filled with reserved fields
  - https://github.com/DmytroLevit/peakrdl-ethercat-xml



# Test Setup


Digital IO terminal
PLC CPU
Asyncronous IO board
EtherCAT FPGA board
X2Timer
NAT-AMC-ZYNQUP-ECAT


PLC9
PLC7
PLC5
PLC3
PLC1

# System Operation

- Board recognized by the TwinCAT software
- Successful data transmission
  - 1 ms cycle time
- Distributed clocks synchronization

| No | Addr | Name | State | CRC | Reg:0910 | Reg:0912 |
|---|---|---|---|---|---|---|
| 1 | 1001 | Box 1 (Single EuXFEL ECAT Project) | OP | 0, 0 | 0xE974 (59764) | 0xD00C (53260) |
| 2 | 1002 | Term 2 (EK1100) | OP | 0, 0 | 0xE967 (59751) | 0xD00C (53260) |
| 3 | 1003 | Term 3 (EL2258) | OP | 0 | 0xE966 (59750) | 0xD00C (53260) |

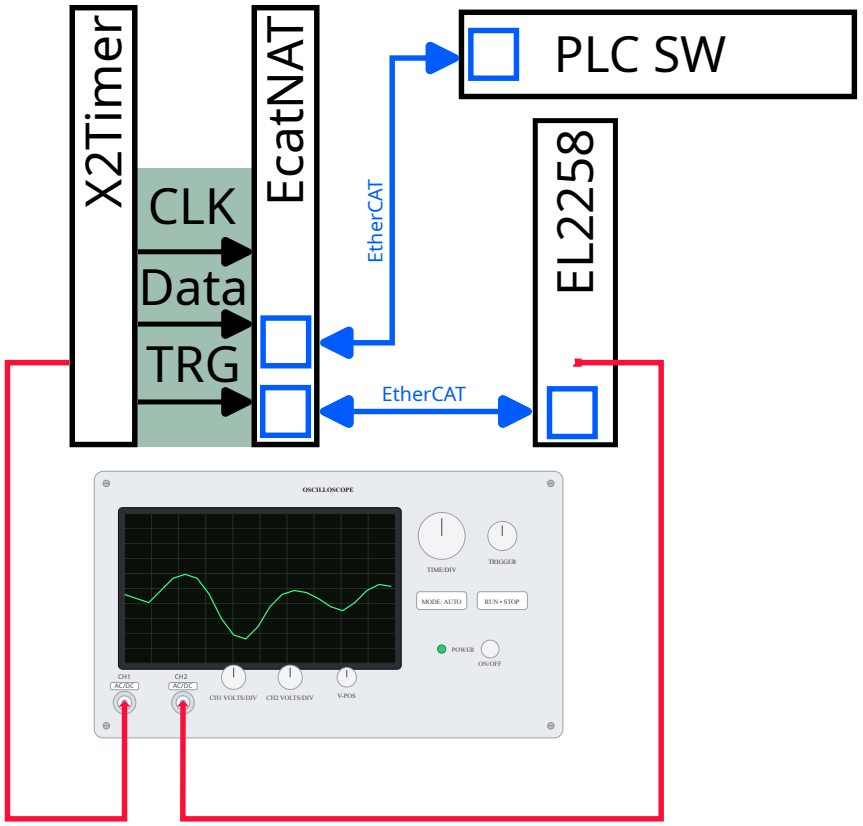
Chain configuration and system clock registers

| ecatnat_pdi | |
|---|---|
| sync | 1 |
| unknown_packet | 0 |
| frame_error | 0 |
| parity_error | 0 |
| crc_error | 0 |
| crc_error_cnt | 1 |
| Reserved_00 | 0x0000 (0) |
| Reserved_01 | 0x0000 (0) |
| Reserved_02 | 0x0000 (0) |
| Reserved_03 | 0x0 (0) |
| trigger_timestamp | 1105784054 |
| trigger_timestamp_s | 1778966345 |
| trigger_timestamp_us | 967769 |
| first_bunch | 40 |
| last_bunch | 40 |
| num_bunches | 1 |
| Reserved_04 | 0x0000 (0) |
| train_id | 2642051039 |
| beam_mode | 0 |
| Reserved_05 | 0x0000 (0) |
| Reserved_06 | 0x0000 (0) |
| fw_date | 335880230 |
| fw_time | 1382673 |
| fw_version | 1005795304 |
| fw_sha | 60239983 |

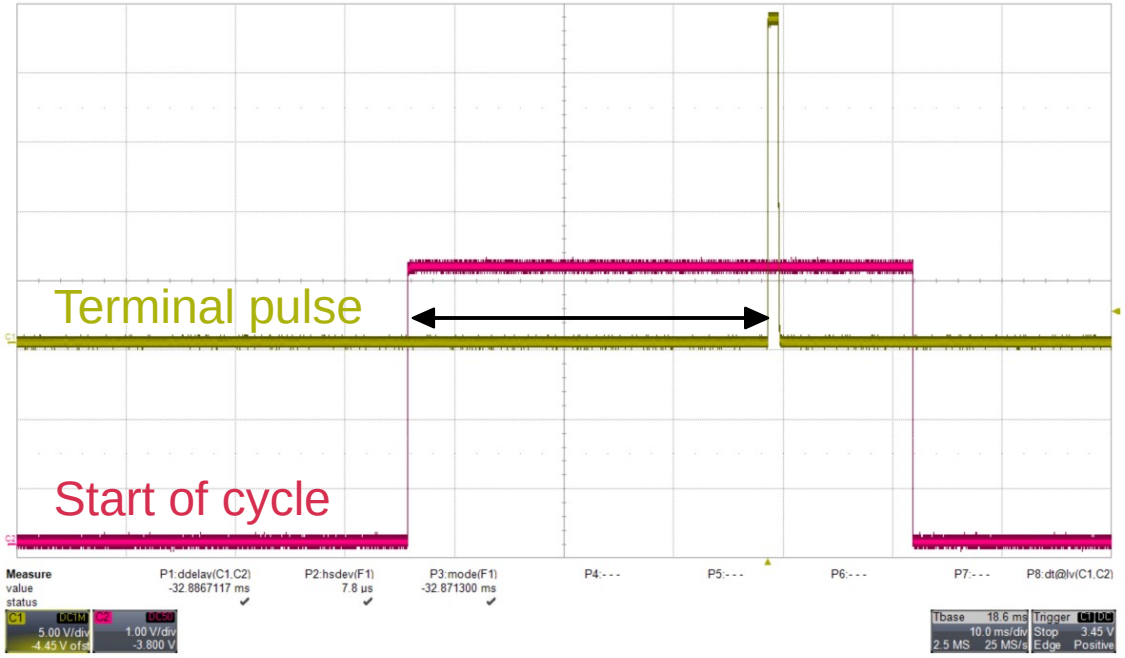
Registers read by TwinCAT

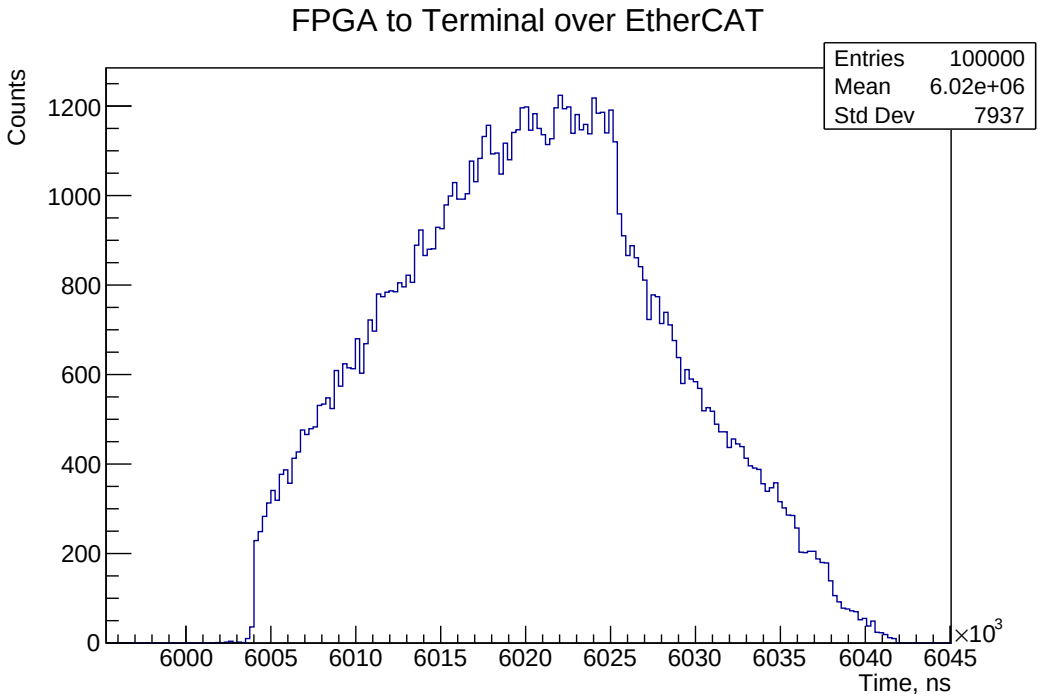
# Synchronization Between Timing System and Terminal

- Trigger from X2Timer
  - Transmit trigger from X2Timer to FPGA board over backplane
  - DC timestamp by the IP core: $\mathbf{t_{trg}}$
- PLC software for pulse generation
  - $\mathbf{t_{pulse}}=\mathbf{t_{trg}}$ + 6 ms
- Pulse difference measurement by oscilloscope



# Synchronization Between Timing System and Terminal

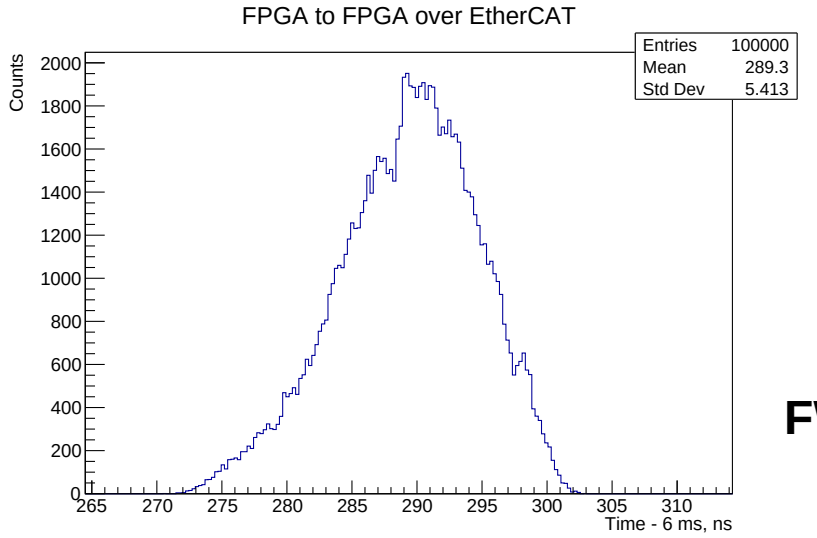


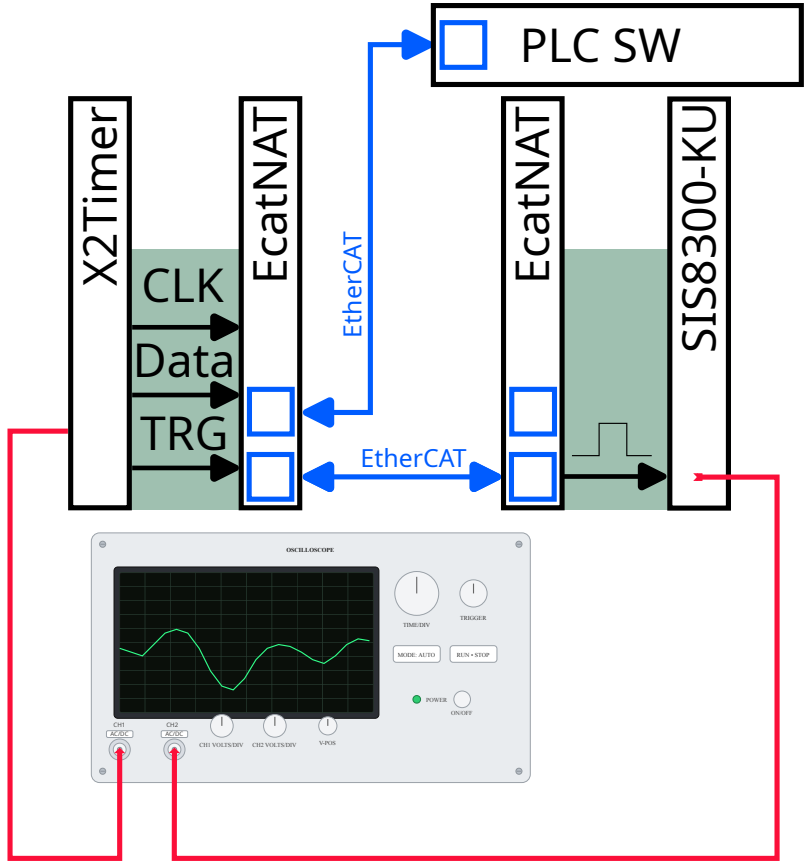

**FWHM = 20 us**

# Synchronization Between Two FPGA Boards

- 2nd FPGA board instead of terminal
  - Generate pulse with the DC timestamp
  - Transmit pulse to X2Timer over backplane
  - Measure time difference:




**FWHM=12.75 ns**



# Example of a Possible Application for PLC and Timing Integration

- Pump-probe measurement of structural evolution of matter at the **FXE** instrument
  - **Optical** excitation pulse to **initiate reaction**
  - **X-ray** pulse to **measure** atomic structure
  - **Delay variation** between both pulses to measure different phases of reaction **O(fs)**
- Optical delay line: **movable retro-reflectors**
  - **100 ps range** (7.5 mm)
- Current measurement cycle:
  - Stop DAQ
  - Change delay
  - Start DAQ

# Example of a Possible Application for PLC and Timing Integration

- Reduce downtime by keeping ODL moving:
  - Measure mirror position at the time trigger arrives at the instrument
  - Repeat experiment to statistically cover full delay range
- Requirements:
  - **3 fs** jitter at **2 mm/s** ODL speed
    - **200 us timing stability**
    - **Requirement for encoder**

# Summary

- Worked together with N.A.T to build FPGA board for EtherCAT communication
- Identified possible applications of the system
  - Desired precision **~200 us**
- Implemented synchronization for the PLC systems using Beckhoff's EtherCAT IP core
  - Precision of **12 ns** is sufficient for PLC applications
- Developed and opensourced peakRDL modules for keeping registers synchronized