

# Optoelectronics & Microelectronics

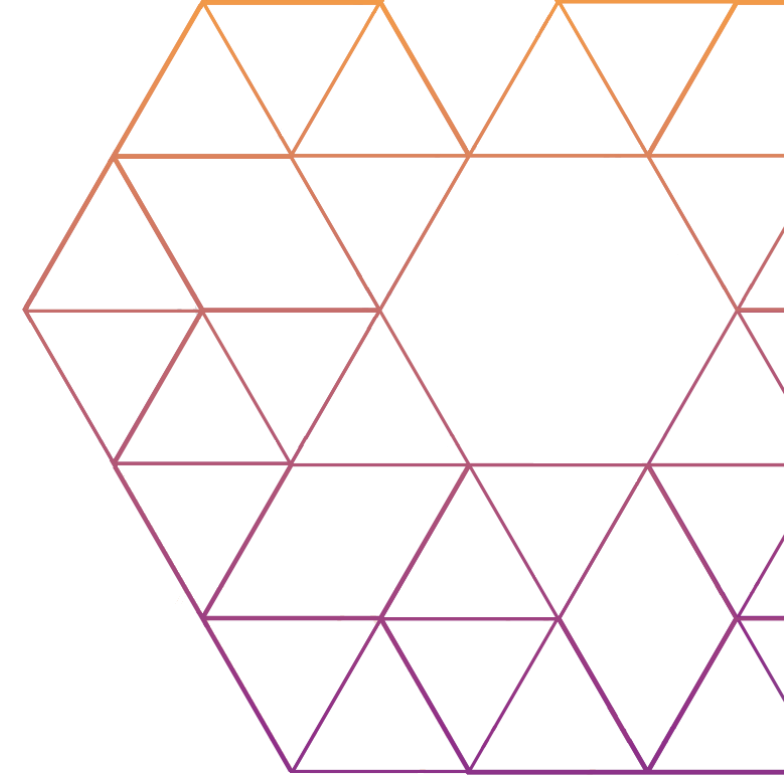
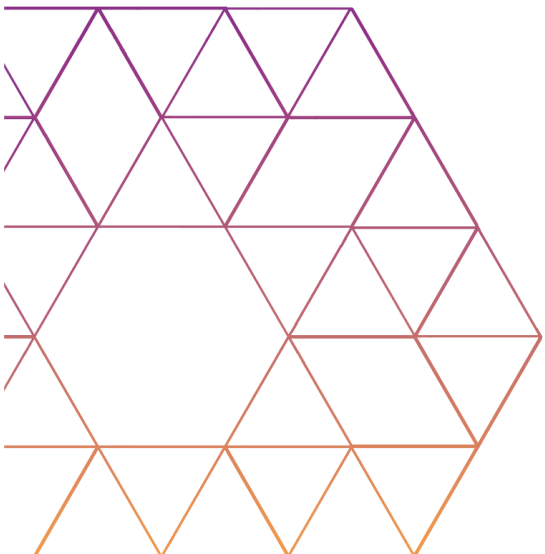
*CERN's unique know-how derived from years of designing, testing and installing microelectronics exposed to harsh environments.*

# CERN's unique position

Design and integration of high performance and extreme radiation tolerant ASICs and optoelectronic modules

Long history of pushing the limits of mixed-mode circuit design for large detector systems

Broad range of testing and qualification capability for radiation hardness of ASICs and optoelectronic modules



Extremely radiation  
tolerant

Up to  
G-rad

Low power  
density

<100  
mW/  
cm<sup>2</sup>

Time tagging  
resolution

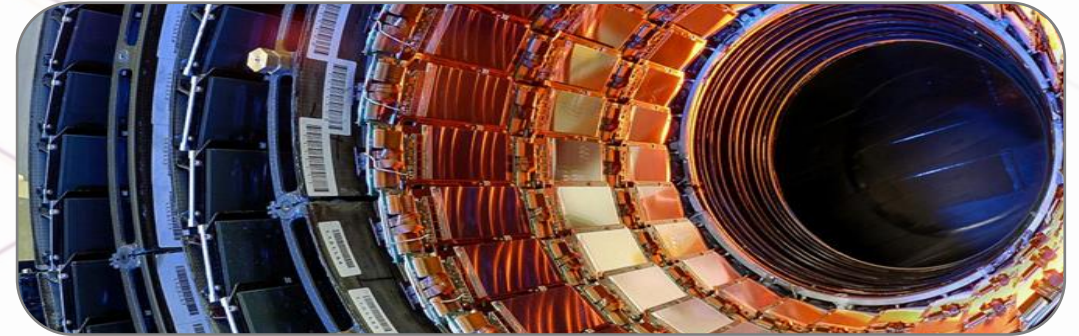
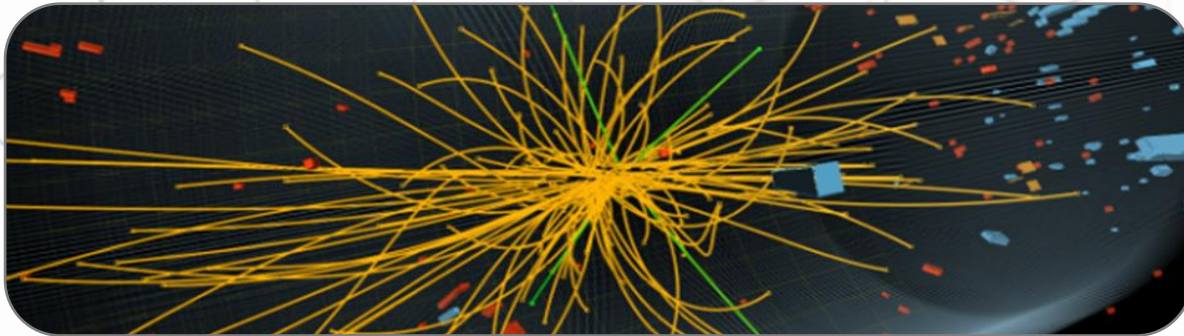
~ 10ps

Number of rad-hard chips  
installed in the LHC

>> 1M

Opto & Micro-  
electronic know-  
how at CERN

# Key competence: Radhard electronics



what

To withstand the level of radiation present in the collision points, unique expertise designing and integrating high performance and extreme radiation tolerant ASICs has been built. Broad range of testing and qualifying capability for radiation hardness of ASICs. Designed in large collaborative team

tech specs

- Expertise on the full range of effects induced by radiation:
  - TID Total Ionising Dose on ASICS behavior
  - Single event effects
  - Displacement damage
- Radhard by design using standard technologies
- Expertise in the testing procedures
- Selection and qualification of COTS (Commercial Off-The-Shelf)

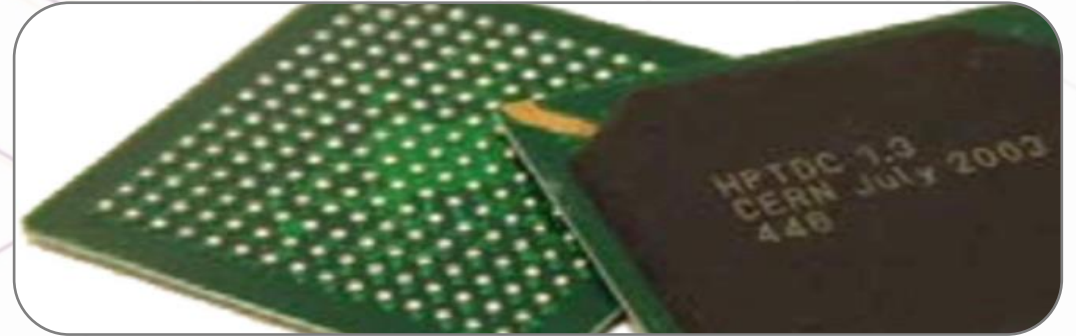
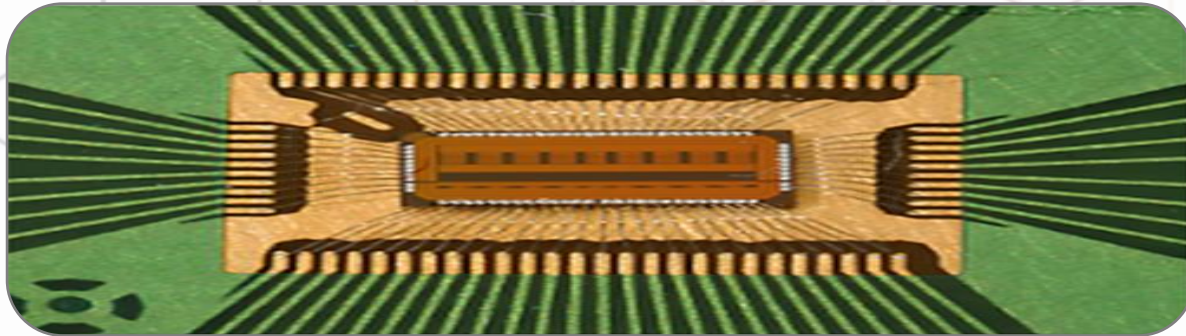
apps

- Medical imaging
- Hadron therapy beam monitoring
- Non-destructive testing
- Aerospace
- Nuclear facilities

added value

- Hands-on radhard design competences  
→ **Know-how to accelerate your radhard design**
- Operating fast and large complex systems composed of thousands of components in ns time precision  
→ **Know-how in building large, ultra fast systems**
- Access to a large database and network of qualified COTS  
→ **Know-how of many radhard components / suppliers**

# Key competence: Mixed-mode electronics



what

At CERN, we need our chips to be extremely reliable (several years of continuous operation) and low maintenance (difficult to access when installed). Therefore, designers are pushing the limits of mixed-mode circuit design for large detector systems with 100 millions of parallel operation channels requiring ns timing synchronisation.

tech specs

- 4 large CERN experiments using mixed mode circuits that proved to work continuously for already 12 years under high radiation with minimum maintenance.
- Power constraints (<100mW/cm<sup>2</sup>)
- ns time precision moving to 100 ps time precision
- Micro spatial resolution

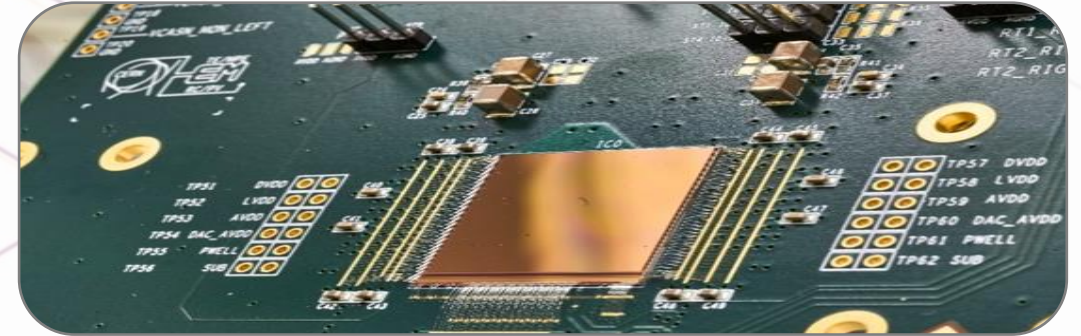
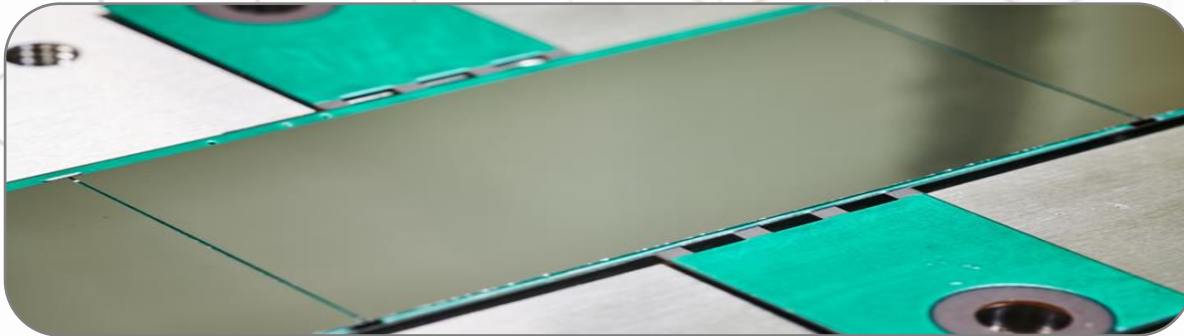
apps

- Medical imaging
- Hadron therapy beam monitoring
- Non-destructive testing
- Aerospace
- Nuclear facilities

added value

- Vast experience with use of mixed-mode electronics in closed and extreme harsh environments  
→ **Know-how on operation of fast systems exposed to radiation**
- Experience with use of multi channel operation designed for minimum maintenance  
→ **Know-how for robust integration and design**

# Key competence: Monolithic pixel chips design



what

Monolithic Active pixel Sensors detectors are high granularity tracking detectors, which provide unambiguous and precise hit information in the harsh environment close to the interaction point. The sensitive volume and part or the full readout circuitry is combined in ONE piece of silicon.

tech specs

Sensor design:

- Timing resolution ns
- Radhard: TID 10s of Mrad

Circuit design:

- Low consumption: 20nA /ampli

Read out architecture:

- High rate: Mega counts /mm<sup>2</sup>/sec

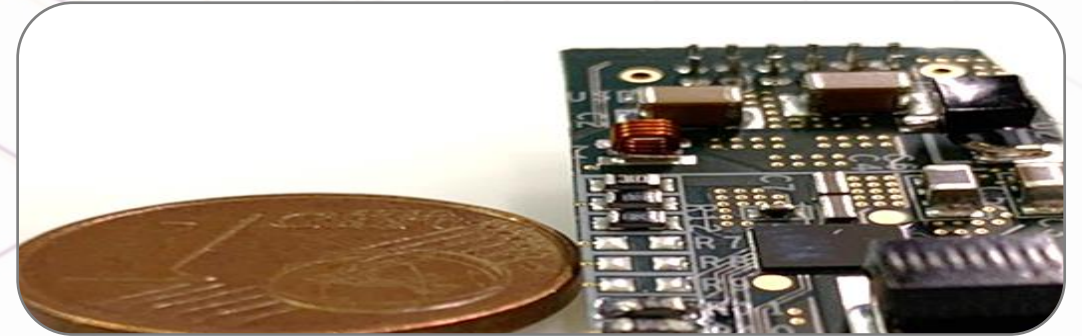
apps

- Proton Computed Tomography
- Particle track reconstruction for space studies
- High speed imaging for low energy X-ray

added value

- Practical, solution oriented know-how  
→ You save time in implementation of new pixel chips
- Know-how of integration of sensors and circuits  
→ Leverage CERN know-how to help simplification and cost reduction of your detector designs.

# Key technology: Robust DCDC converters



what

At CERN, we need DCDC converters in places with high magnetic fields and high radiation levels. Therefore we design and manufacture fully integrated magnetic field and radiation tolerant DCDC Point-Of-Load (POL) converters, enabling distribution at a higher voltage and lower current inside the detector.

tech specs

- Input voltage 2.5 or 12V
- Continuous 4A load capability
- Switching frequency in the range of 1 to 4 MHz
- Synchronous Buck topology with continuous mode operation.
- High bandwidth feedback loop for good transient performance.
- Radiation tolerant:
  - TID upto >200Mrad(Si).
  - Displacement damage up to  $2 \times 10^{15}$  N/cm<sup>2</sup>
  - Single event effects immunity

apps

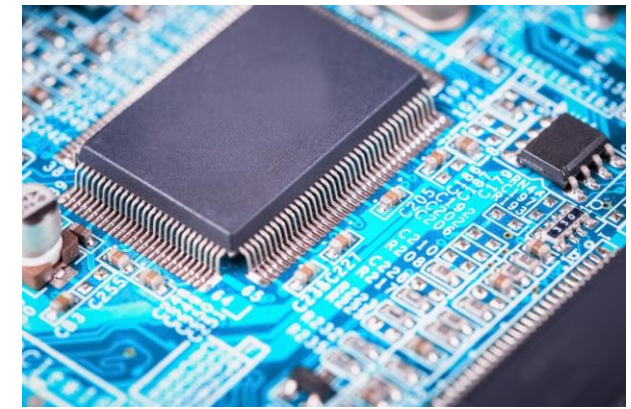
Power distribution where radiation and magnetic field tolerance is required such as: Avionics, Space, Safety, Medical equipment, Electric transportation

added value

- DCDC converters designed to operate in magnetic and/or radiation environments  
→ **Increase reliability and robustness**
- Fully integrated, compact, high density designs  
→ **Suitable for applications with limited space**

# DC-DC Converters

A radiation and magnetic field tolerant DC-DC Point-Of-Load (POL) enables distribution at higher voltage with local on-detector conversion to the voltage required by the electronics, considerably decreasing the current in the cables.



## **bPOL12V**

- Input voltage 5.5 to 12 V
- Continuous 4 A load capability
- Adjustable switching frequency 1-3 MHz
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150 kHz) for good transient performance
- Protection Over-Current (OVC) and Over-Temperature (OTP)
- Protection Input Under Voltage Lock Out (ULVO)
- Radiation tolerant: TID up to >150 Mrad(Si)
- **bPOL12V also available as a standalone licensable ASIC**

### **APPLICATIONS**

- Point Of Load in distributed power systems where either radiation tolerance or magnetic field tolerance, or both, are required.

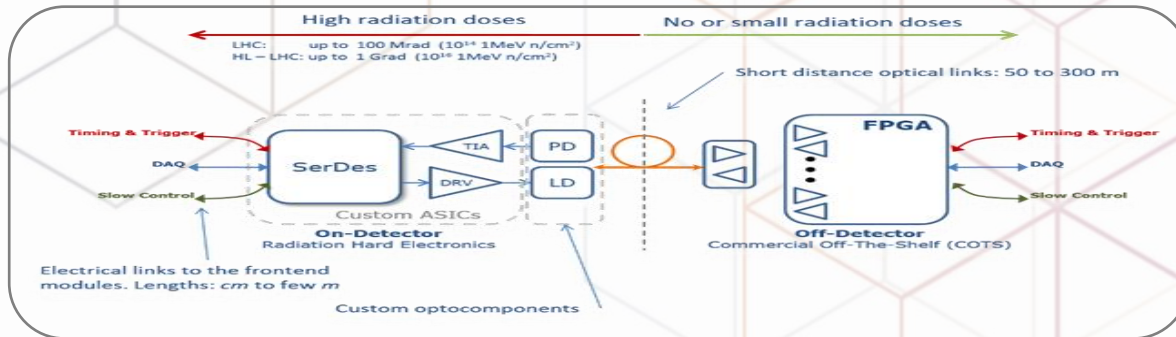
## **bPOL48V**

- Input voltage 17 to 48 V
- Output current up to 10 A
- Integrated 5 V and 12 V regulators for the power stage
- Adjustable switching frequency 0.5-3 MHz
- High bandwidth feedback loop (100 kHz) for good transient performance
- Protection Input Under-Voltage Lock Out (ULVO) and Over-Temperature (OTP)
- Radiation tolerant: TID up to > 50 Mrad(Si)
- **GaN-based power stage (also available as a standalone licensable ASIC)**

### **APPLICATIONS**

- Point Of Load in distributed power systems where radiation tolerance is required.

# Key technology: High speed optical links



what

In CERN experiments, inner tracking detectors require low-mass, high speed radiation tolerant optical links to read out data from the detectors and to send synchronisation signals and commands to the detectors.

tech specs

- Rad hard: 1MGy total dose
- Wide temperature range : -35°C to 65°C
- Fast and bi-directional: 2.56 Gb/s in the downstream towards the detector; and 5.12 or 10.24 Gb/s in the upstream away from the detector
- Compact optical transceiver : 1 transmitter and up to 4 receivers
  - 20 mm x 10 mm x 2.5 mm

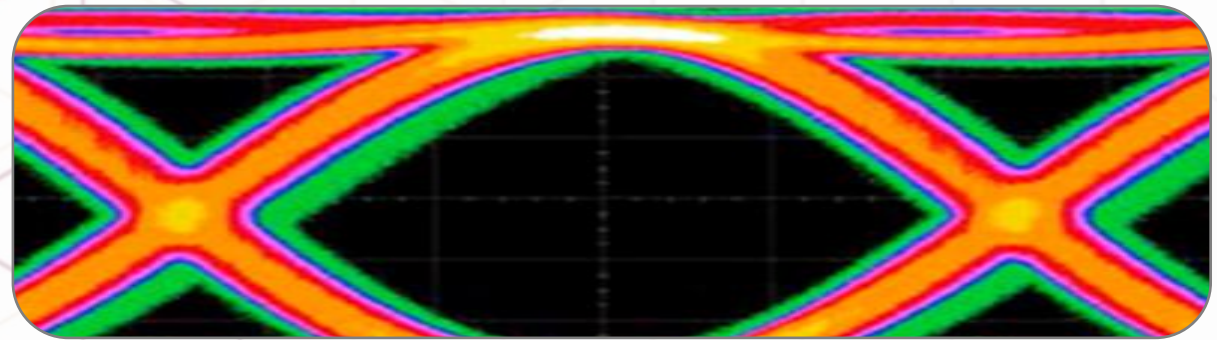
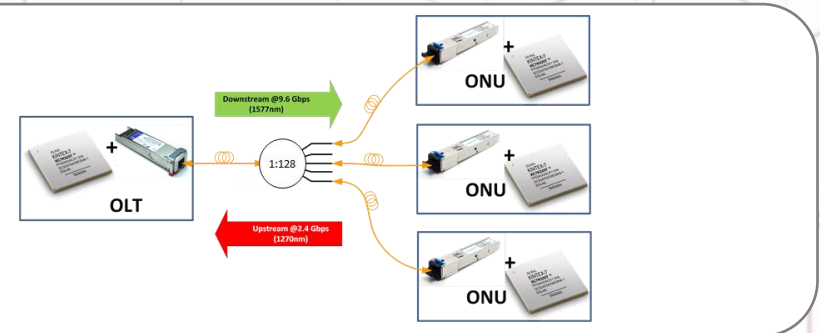
apps

- Aerospace
- Safety
- Nuclear power plants

added value

- Compact  
→ Suitable where little space is available
- Radhard  
→ Designed for harsh environment
- High speed:  
→ Transfers large amount of data

# Key Technology: Timing, trigger and control system



what

In the LHC experiments at CERN, the Timing, Trigger and Control (TTC) system is responsible for delivering the TTC commands from the central processor to the detector sub-partitions. The TTC-Passive Optical Network (PON) project was born from the idea of making use of the well-developed by the telecom industry FTTx/PON technology to propose an upgrade to the current off-detector TTC system, overcoming some of its limitations.

tech specs

- Network:
  - Wavelength multiplexing
  - Passive network, split ratio up to 1:128
  - Network status online monitoring (current, optical power, eye diagram, propagation time)
- Downstream:
  - ~10Gbps
  - Stability < 10ps rms
  - Low latency
  - BER < 10<sup>-12</sup>
- Upstream:
  - Time Domain Multiplexing
  - No arbitration
  - Short GAP between bursts
  - Downstream synchronous

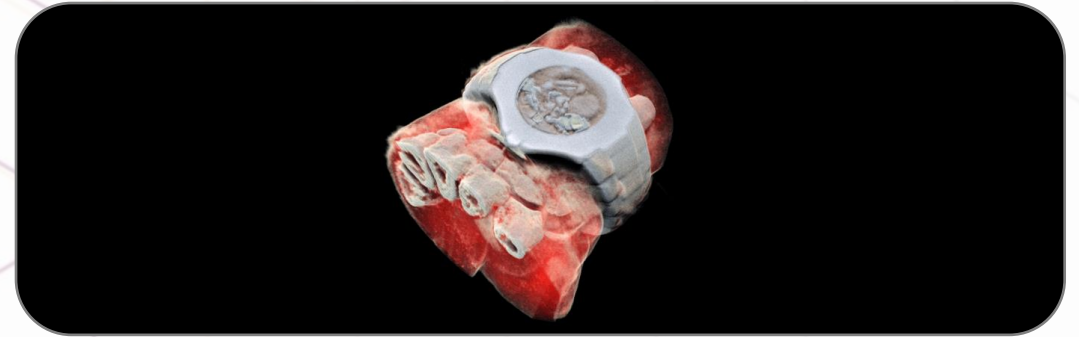
apps

- Telecommunications
- Clock Distribution Networks

added value

- High Split Ratio
  - up to 128 nodes
- Very short gaps between upstream frames (25ns)
  - maximizing total bandwidth upstream
- Extremely stable and robust against line errors
  - <10ps rms and Forward Error Correction scheme
- Complete Online Monitoring:
  - continuous tracking of network status
  - predictive maintenance

# Key technology: Medipix chip family



what

A family of pixel detector read-out chips for particle imaging and detection developed by a consortium lead by CERN. Medipix works like a camera, detecting and counting each individual particle hitting the pixels. This enables high-resolution, high-contrast, noise hit free images. The Medipix chip family aims at frame based imaging and spectroscopic x-ray imaging.

tech specs

- Charge summing and allocation scheme – mitigating charge sharing
- 2 thresholds per 55µm pixel each with 5 bits of local adjustment
- High gain mode (HG, lower linearity, lower noise) or low gain mode (LG)
- Configurable counter depths: 2 x 1-bit, 2 x 4-bit, 2 x 12-bit, 1 x 24-bit
- Continuous or sequential data acquisition and readout

apps

- Medical imaging
- Electron Microscopy
- Non-destructive testing
- Particle track reconstruction

added value

- Colour imaging  
→ Detect various components
- Designed for particle tracking  
→ Very high resolution
- Can be used on wide range of detection devices  
→ Very broad applicability

# Key technology: Timepix chip family



what

By using ASICs that can accurately measure time, one can directly reconstruct the 3D track of passing charged particles. Timepix is a family of pixel detector read-out chips for particle imaging and detection developed by a consortium lead by CERN. The Timepix family is designed for detection with nanosec resolution with a data driven architecture (last version).

tech specs

- Two main measurement modes: (1) simultaneous 10 bit ToT and 18 bit TOA and (2) 10 bit event counting and 14 bit integral TOT
- TOT monotonic for large positive charges
- Fast TOA for time stamping with a precision of 1.56 ns
- Data driven readout: dead time free, for a maximum hit rate of 40 Mhits/s/cm<sup>2</sup>
- Shutdown/wake-up features for power pulsing tests on a full system

apps

- Electron Microscopy
- Particle track reconstruction

added value

- Designed for particle tracking  
→ **High resolution**
- Can be used on wide range of detection devices  
→ **Very broad applicability**



		Timepix2	Timepix3	Timepix4	
Tech. node (nm)		TSMC 130	IBM 130	TSMC 65	
Year		<b>2018</b>	<b>2013</b>	<b>2019</b>	
Pixel size ( $\mu\text{m}$ )		55	55	55	
# pixels (x x y)		256 x 256	256 x 256	448 x 512	
Sensitive area		<b>1.98 cm<sup>2</sup></b>	<b>1.98 cm<sup>2</sup></b>	<b>6.94 cm<sup>2</sup></b>	
Number of sides for tiling using WB		3 (85.6% active area)	3 (86.7% active area)	2 (93.7% active area)	
Number of sides for tiling using TSV		<b>3 (85.6% active area)</b>	<b>3 (91.6% active area)</b>	<b>4 (99.3% active area)</b>	
Front-end	positive (h <sup>+</sup> )	High Gain (25mV/kh <sup>+</sup> ) Logarithmic Gain (19mV/kh <sup>+</sup> )	High Gain (45mV/kh <sup>+</sup> ) (Volcano >0.3MeV/pixel)	High Gain (35mV/kh <sup>+</sup> ) Low Gain (20mV/kh <sup>+</sup> ) Logarithmic Gain	
	negative (e <sup>-</sup> )	High Gain (25mV/ke <sup>-</sup> )	High Gain (45mV/ke <sup>-</sup> )	High Gain (35mV/ke <sup>-</sup> ) Low Gain (20mV/ke <sup>-</sup> )	
Minimum detectable charge		~600 e <sup>-</sup>	~500 e <sup>-</sup>	~500 e <sup>-</sup>	
Operation Modes	Tracking (Event arrival time and/or energy)	Readout	<b>Full Frame-based (Sequential or Continuous R/W)</b>	<b>Data-driven (48-bit packet per pixel hit)</b>	<b>Data-driven (64-bit packet per pixel hit)</b>
		Event Data	TOT and TOA; TOT or TOA	TOT & TOA	TOT & TOA
		TOT energy resolution	<b>~0.75keV (FWHM Si)</b>	<b>~2KeV (FWHM Si)</b>	<b>~1KeV (FWHM Si)</b>
		TOA bin size	<b>10ns (@100MHz)</b>	<b>1.56ns (On-pixel TDC @40MHz)</b>	<b>195ps (On-pixel TDC @40MHz)</b>
		TOA dynamic range	2.62ms (@100MHz)	409.6 $\mu\text{s}$ (14b@40MHz)	1.63ms (16b@40MHz)
		Max Rate	<1x10 <sup>6</sup> hits/cm <sup>2</sup> /s	43x10 <sup>6</sup> hits/cm <sup>2</sup> /s	358x10 <sup>6</sup> hits/cm <sup>2</sup> /s
	Max Pix Rate	33 Hz/pixel	1.3 KHz/pixel	10.8 KHz/pixel	
	Imaging (Event counting)	Readout	<b>Full Frame-based (Sequential or Continuous R/W)</b>	<b>Zero-suppressed (with pixel addr) (Sequential R/W)</b>	<b>Full Frame-based (Continuous R/W)</b>
		Counter depth	10-bit or 14-bit	Counting (10-bit) or iTOT (14-bit)	8-bits or 16-bits
		Frame rate	<b>4.9 kfps @10-bit 32x100Mbps 3.5 kfps @14-bit 32x100Mbps</b>	<b>1.62 kfps @48-bit 8x640Mbps</b>	<b>89.2 kfps @8-bit 16x163Gbps 44.8 kfps @16-bit 16x163Gbps</b>
		Max Count Rate	~35 x 10 <sup>9</sup> hits/cm <sup>2</sup> /s	~82 x 10 <sup>9</sup> hits/cm <sup>2</sup> /s	~800 x 10 <sup>9</sup> hits/cm <sup>2</sup> /s
	Maximum Readout bandwidth		3.2Gbps (32 x 100MHz)	≤5.12Gbps (8x SLVS@640 Mbps)	≤163.84Gbps (16x @10.24 Gbps)
Power consumption		450mW/cm <sup>2</sup> (nominal) 165mW/cm <sup>2</sup> (low power mode)	625mW/cm <sup>2</sup> (nominal) 108mW/cm <sup>2</sup> (low power)	700mW/cm <sup>2</sup> (nominal) 200mW/cm <sup>2</sup> (low power)	
Paper		<a href="https://www.sciencedirect.com/science/article/pii/S1350448719305165">https://www.sciencedirect.com/science/article/pii/S1350448719305165</a>	<a href="https://iopscience.iop.org/article/10.1088/1748-0221/9/05/C05013">https://iopscience.iop.org/article/10.1088/1748-0221/9/05/C05013</a>	<a href="https://www.sciencedirect.com/science/article/pii/S0168900222007811">https://www.sciencedirect.com/science/article/pii/S0168900222007811</a>	

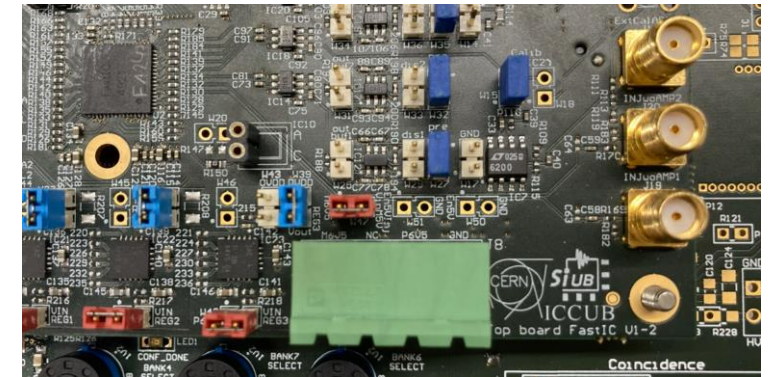
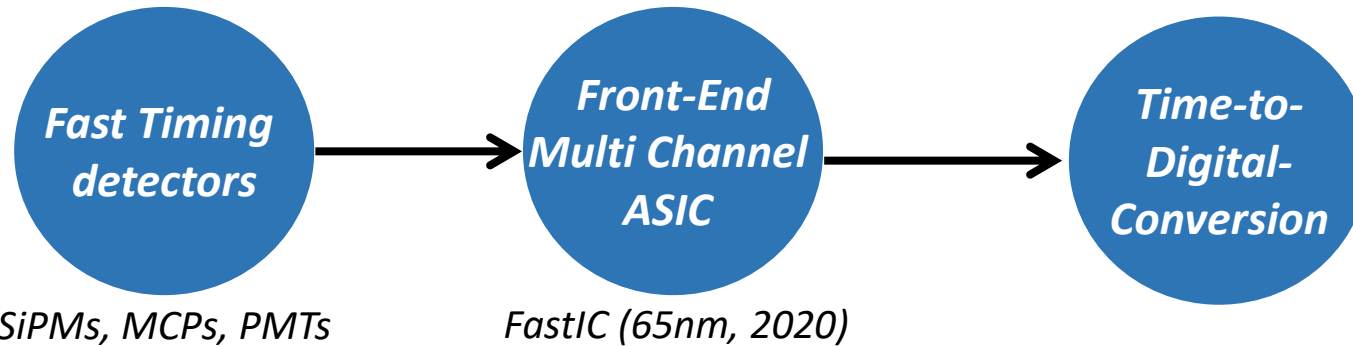
- Hybrid pixel detectors were developed to respond to a need at the LHC: particle tracking in high rate environments.
- Single particle counting detectors have been widely used in education, space science, materials analysis and X-ray applications

# FastIC+



FastIC (65nm CMOS) is a chip for the **read-out of fast radiation detectors** providing **particle time of arrival and energy** information. The chip has applications in medical and biomedical fields, e.g. for

**Time-of-Flight Positron Emission Tomography (PET), mass spectrometry or fluorescence detection in biological samples.**



- Multichannel readout ASIC that has incorporated a fast front-end, discriminators and analog signal processing chain and a Time-to-Digital (TDC) with a **time bin of 25ps**.
- Enables **compact system integration** and **low power consumption**.
- Singled ended, differential & summation of 4 single-ended channels (+/-) to explore benefits of segmentation of detector areas;
- Large range of input capacitances;
- Large dynamic range (with positive and negative polarity readout).

**To the best of our knowledge FastIC+ is the first digital readout ASIC achieving  $\text{ctr} < 100\text{ps fwhm}$**

# FastIC+

Parameter	Value
Technology	65 nm CMOS TSMC
Power consumption	~ 12 mW/ch in SE mode ( $V_{DD} = 1.2$ V), depends on operation mode (~ 3 mW/Input Stage). Non-Linear ToT 6 mW/ch.
Input voltage	Adjustable input node DC voltage.
Number of channels	Input channel configuration (current mode processing): 8 Single Ended (SE) or 4 Differential (DIFF).
Connection Type	Configurable SE (Pos/Neg polarity), DIFF, Sum of 4 (Pos/Neg polarity)
Electronics Time Jitter	~ 30 ps <sub>rms</sub> SPTR (330 pF 3x3 SiPM, LCT5 S13360 SiPM, $V_{ov} = 4.5$ V, $L = 1.2$ nH)
Energy Resolution	Linear (~ 2.5 % Linearity error)
Dynamic Range	The linear energy measurement has 10-bit dynamic range up to ~25 mA of input current.
Maximum Rate	~ 2 MHz (Linear ToT readout) > 50 MHz (Non-linear ToT. Pulse-shape-dependent)
Testing and Calibration	Yes
Interface	I2C
Output	Configurable Digital (single-ended CMOS or differential SLVS) or Analog output (10 pF load).

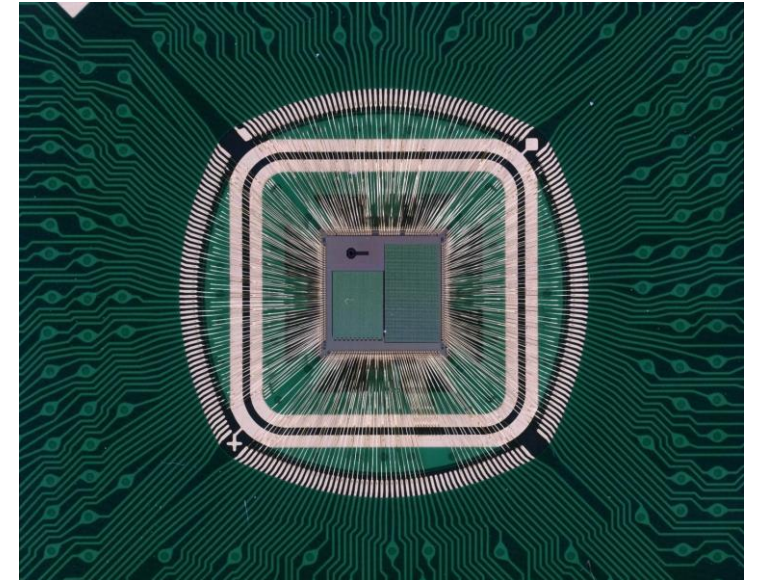
**Paper:** <https://arxiv.org/abs/2506.11655>

# PicoTDC

High performance time to digital converter ASIC chip for use in applications requiring precise time-tagging of electronic signals. E.g. electron and photon detection in medical imaging, laser ranging, life science or material research.

<b>Technology</b>	CMOS 65 nm
<b># Channels</b>	64 or 32 differential channels.
<b>Time binning</b>	3 ps or 12 ps (programmable), <i>with very low jitter (&lt;1ps) and high stability (~1ps).</i>
<b>Reference</b>	40 MHz
<b>Dynamic range</b>	204 $\mu$ s (13 bit @ 40 MHz)
<b>Power</b>	~1.5 – 0.5 W

- Large on-chip data buffering capability.
- Option of triggering with programmable latency and time window.
- Support for overlapping trigger windows.
- Option of using channel 0 as timing channel and trigger generator channel.



## Paper:

PicoTDC: a flexible 64 channel TDC with picosecond resolution <https://doi.org/10.1088/1748-0221/18/07/P07012>

## Tech Brief:

[https://kt.cern/sites/default/files/technology/picotdc/tech-brief/picotdc\\_0.pdf](https://kt.cern/sites/default/files/technology/picotdc/tech-brief/picotdc_0.pdf)