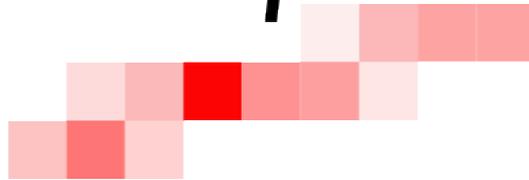


smartpixels



Jennet Dickinson
HFCC Monthly Meeting
June 5, 2025

What is smart pixels?

- Using **machine learning** to perform physics-motivated **data reduction** within the pixelated area of an ASIC
- Our focus so far has been on the LHC
 - Challenge of managing pixel detector data: high rate + many channels
 - Can we shrink the pixel data on-ASIC and send it in the first level of selection?
- Many potential applications at **future colliders**
 - Including Higgs Factories!

Initial motivation

- Silicon trackers at the LHC produce **too much data** to process at the collision frequency of 40 MHz
- The data from these detectors is only read out for triggered events
- **This limits our physics reach.**

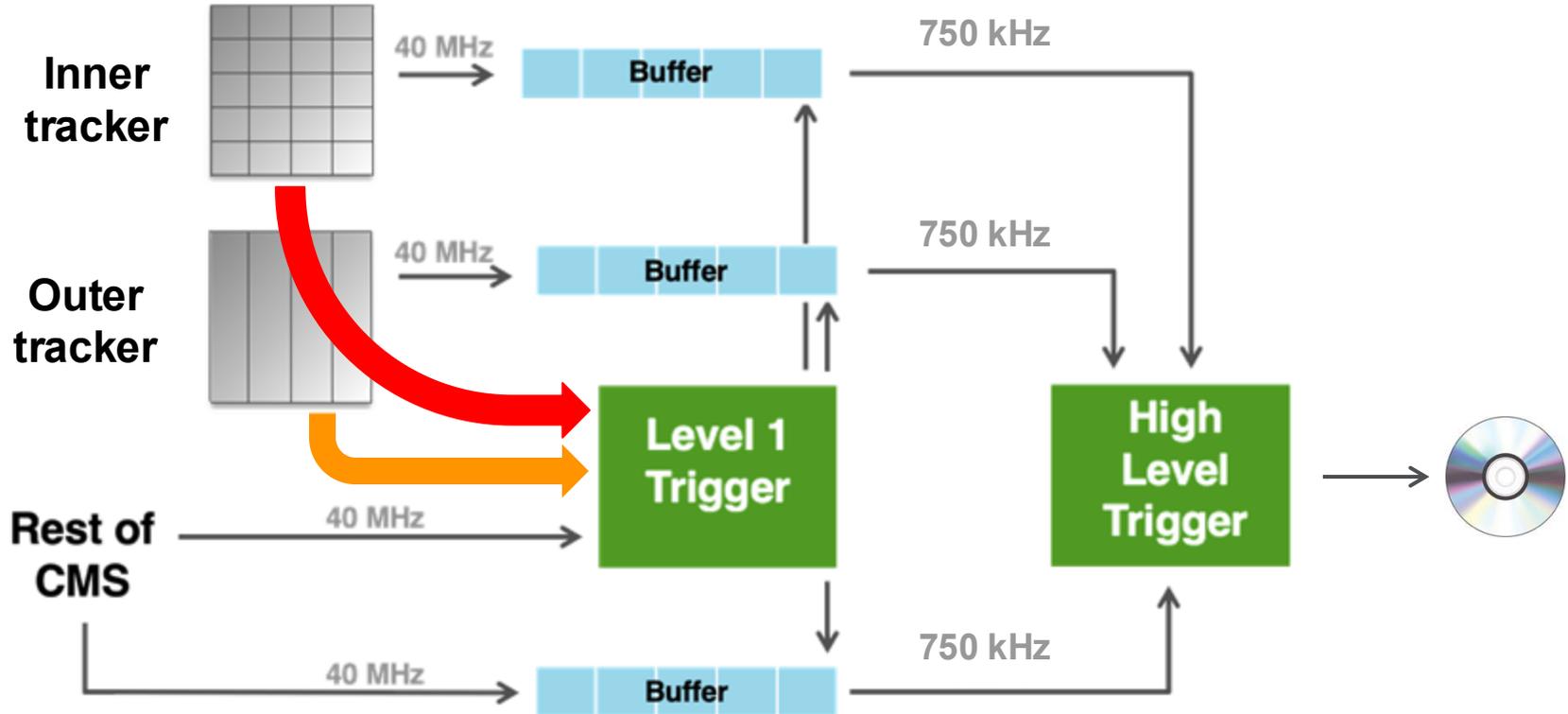


Hadronic
Higgs decays

???

Long-lived
particles

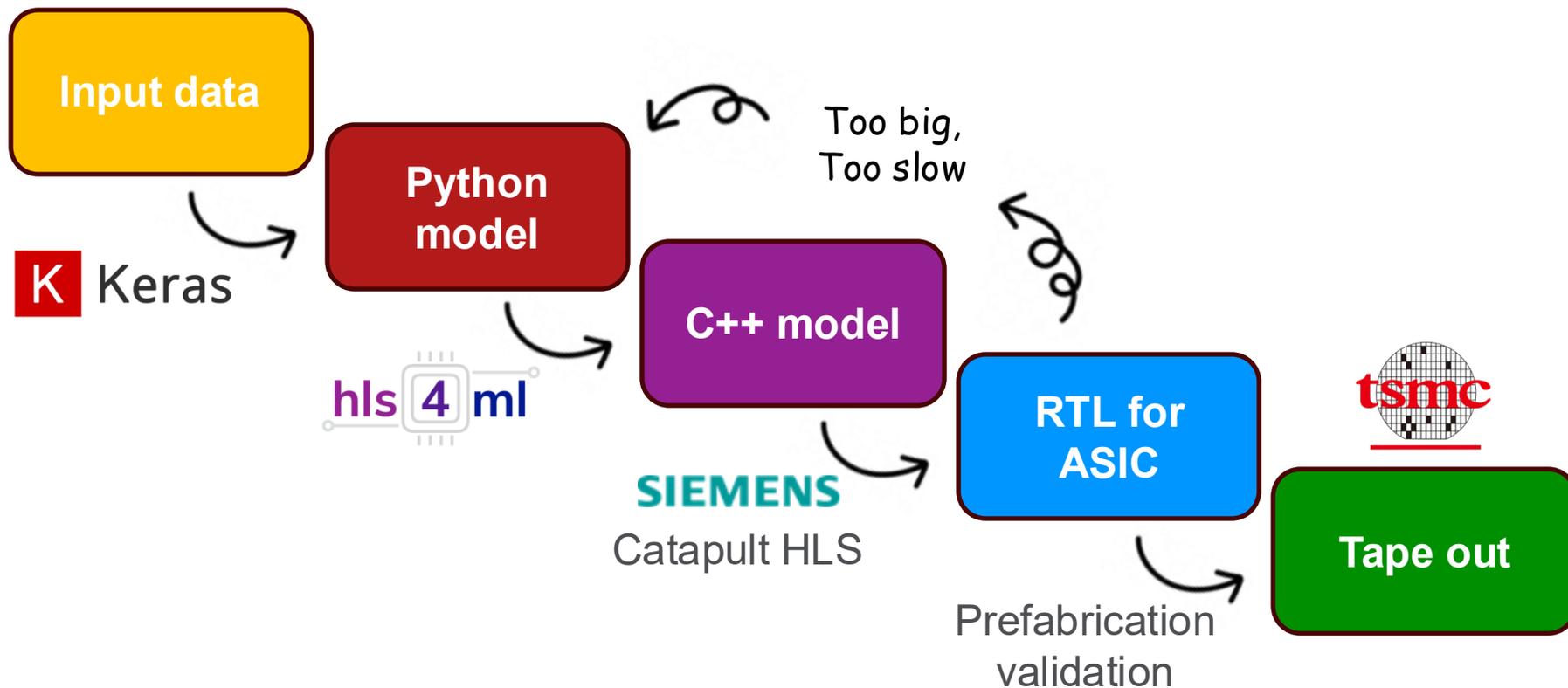
The trigger we dream of



The smart pixels approach

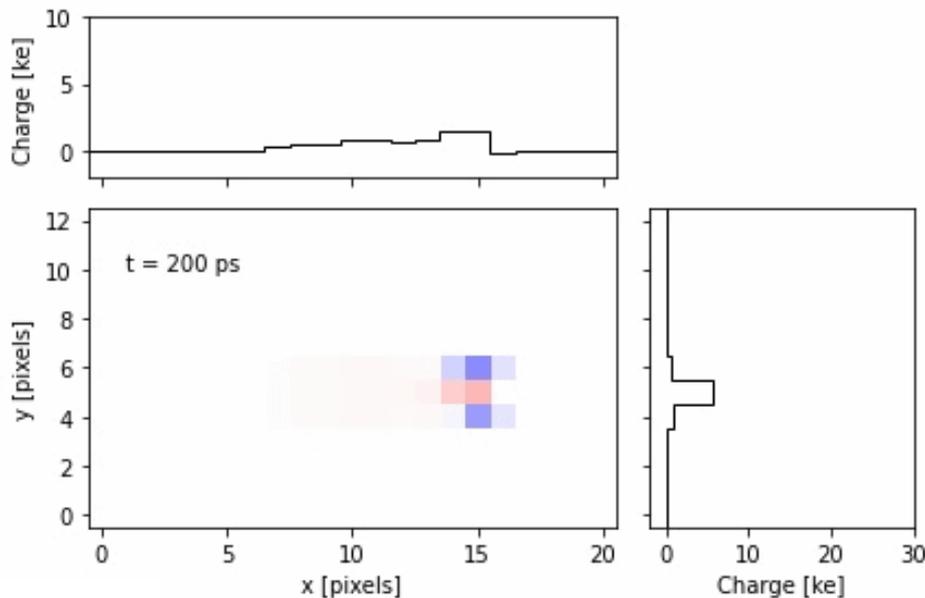
1. **Simulate** charged particle interactions in a silicon detector
2. Develop a **ML algorithm** that reduces data size while capturing the physics content. Algorithms must remain **compact** and **low power**
3. Implement the algorithm in pixelated area of an **ASIC**
4. Tape out and **test** the ASIC

Hardware design flow



Simulation

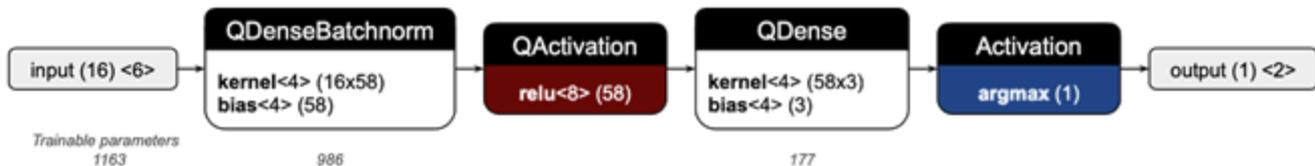
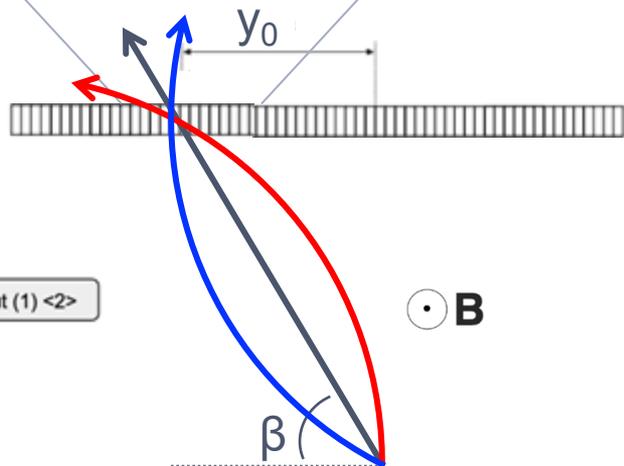
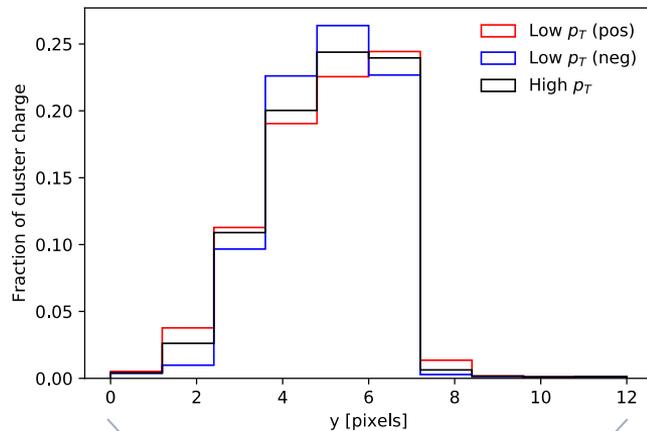
- Dataset for developing algorithms for implementation on-ASIC ([link](#))
Initial conditions taken from tracks in CMS Run 2 data, down to $p_T \sim 100$ MeV
- Simulated interactions π^+/π^- in an array of 13 x 21 pixels
 - Varying pixel pitch, thickness
 - Located at radius of 30 mm
 - 3.8 T magnetic field
 - Time steps of 200 picoseconds



Can we sample that fast?

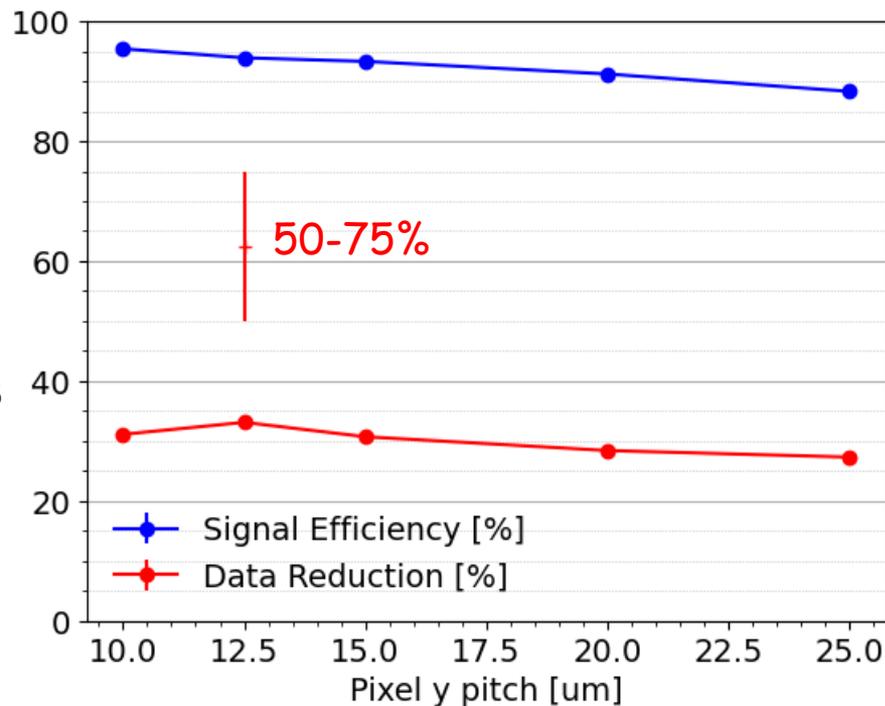
ML model: the p_T filter

- Partition dataset into three classes:
 - Negative charge, $p_T < 200$ MeV
 - Positive charge, $p_T < 200$ MeV
 - Any charge, $p_T > 200$ MeV
- Input features: charge cluster projected onto the y-axis



Performance of the p_T filter

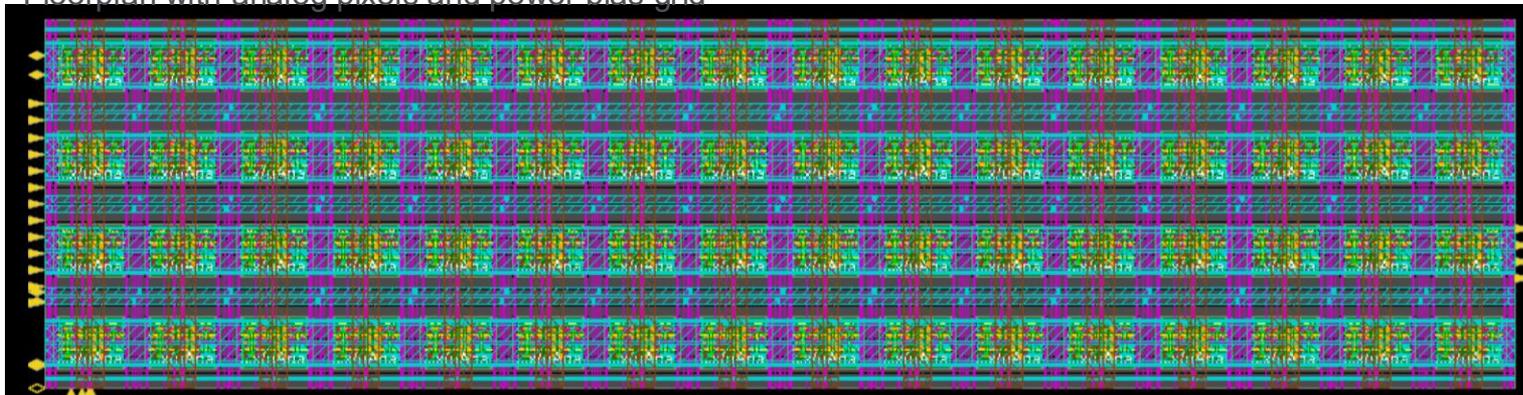
- **Signal efficiency** =
$$\frac{\# \text{ clusters}[p_T^{\text{true}} > 2 \text{ GeV }] \text{ kept}}{\# \text{ clusters}[p_T^{\text{true}} > 2 \text{ GeV }]}$$
- **Data reduction** =
$$\frac{\# \text{ clusters rejected}}{\# \text{ total clusters}}$$
 - Known underestimate: CMS tracks as a starting point \rightarrow a lot was already rejected



Read out integrated circuit

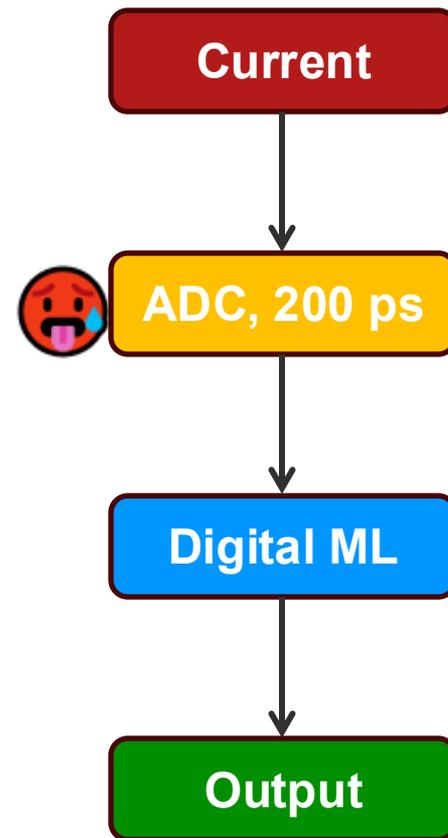
- Synthesized in 28nm CMOS with **reprogrammable NN weights**
 - Area < 0.2 mm², expected to operate at < 300 μW
- Chip is taped out and testing is underway!
 - At Fermilab, Cornell, and UChicago

Floorplan with analog pixels and power bias grid



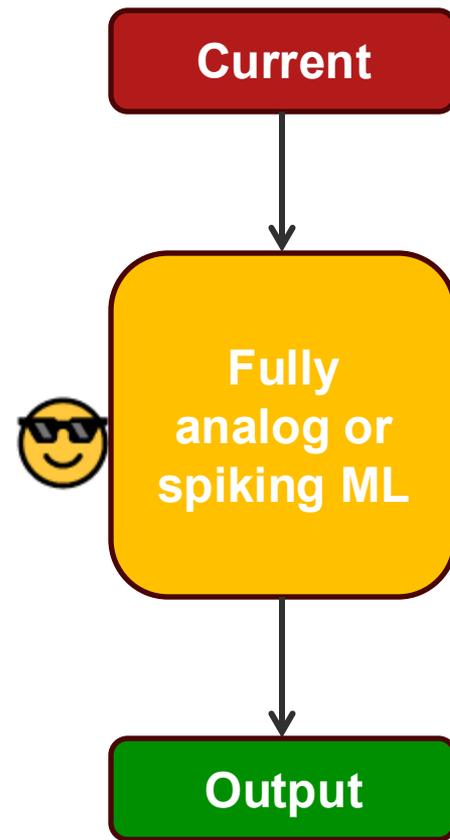
Accessing the pulse evolution

- An ADC that samples at 200ps would require way too much power
 - Can we get good performance sampling at a **lower rate**?



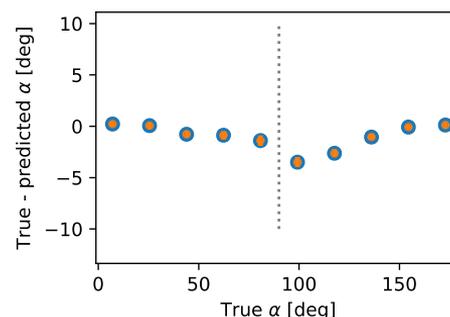
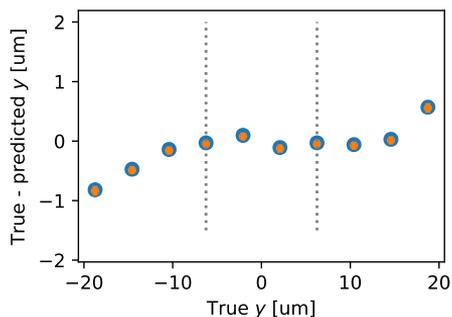
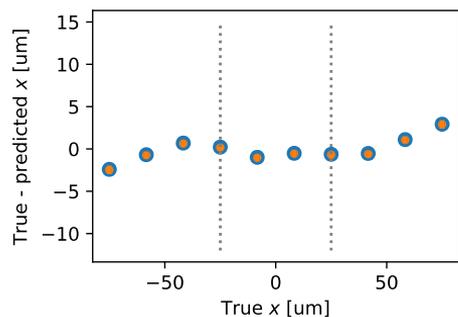
Accessing the pulse evolution

- An ADC that samples at 200ps would require way too much power
 - Can we get good performance sampling at a **lower rate**?
- Can we preserve the timing information using a **spiking or analog** network?
 - Very low power! Helps minimize **thermal load / material budget** in an e^+e^- tracker
 - SNN studies so far: [2307.11242](https://arxiv.org/abs/2307.11242)



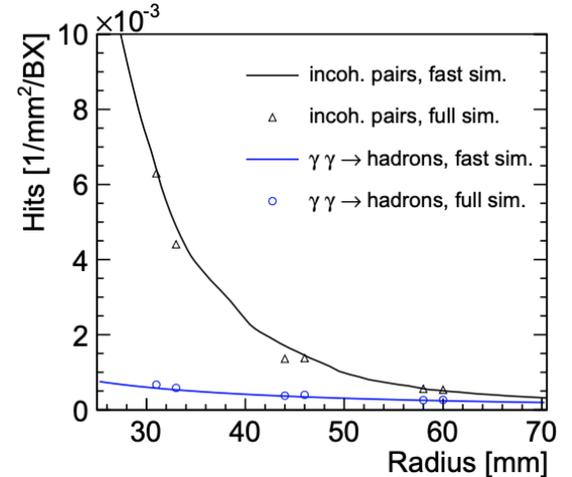
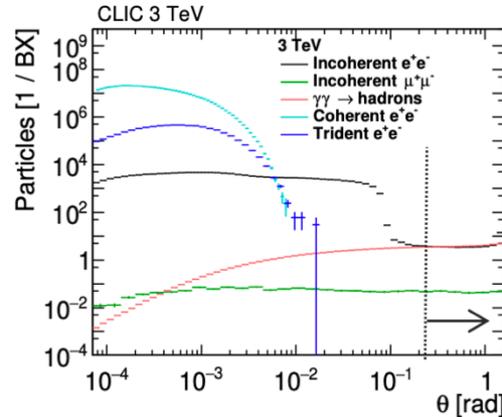
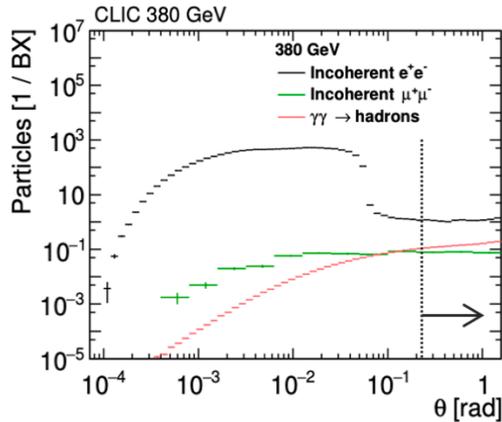
A heftier ML model: feature regression

- Predict and read out the traversing particle's **hit position** and **incidence angle**, plus **uncertainties** (or some subset)
 - A first demonstration from the ML side: [2312.11676](https://doi.org/10.2312/11676)
- Each charge cluster corresponds to the same amount of data
 - **Size of data buffer, volume of data cables** are **independent of geometry** (pixel pitch, sensor thickness)



A word about rate in e^+e^-

- **Beam backgrounds** = very forward particles
 - Factor in choosing the **innermost radius** of the tracking detector
 - Cause high **data rates** in e.g. FCC-ee Z-pole running
- Removing hits from beam background relieve some pressure
 - Train an on-ASIC classifier to filter out small θ

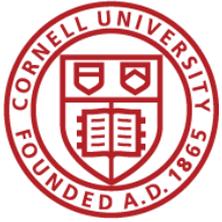


Summary

- On-chip intelligence has great potential to **enhance the physics output** of collider experiments
 - Focus so far has been on LHC experiments
- A **p_T filtering chip** has been designed, taped out, and is being tested
- Touched on some ideas for applications at an e^+e^- Higgs Factory
 - Could allow flexibility for some **critical design choices** (inner radius, pixel pitch)
 - **Emerging technologies** will be critical to minimize material budget / thermal load
 - Analog and neuromorphic / spiking networks, monolithic detectors, 3D stacking

Thank you to the smart pixels team

- **Cornell University** Jennet Dickinson, Ben Weiss, Albert Zhou, Sid Ahuja
- **Fermilab:** Douglas Berry, Giuseppe Di Guglielmo, Farah Fahim, Abhijith Gandrakota, Lindsey Gray, Jim Hirschauer, Ron Lipton, Benjamin Parpillon, Chinar Syal, Nhan Tran
- **Johns Hopkins University:** Petar Maksimovic, Morris Swartz
- **Oak Ridge National Laboratory:** Shruti Kulkarni, Aaron Young
- **Purdue University:** Mia Liu, Arghya Ranjan Das, Shiqi Kuang
- **University of Chicago:** Karri DiPetrillo, Anthony Badea, Eliza Howard, Daniel Abadjiev
- **University of Colorado Boulder:** Keith Ulmer, Jannicke Pearkes
- **University of Illinois Chicago:** Corrinne Mills, Danush Shekar, Mohammad Abrar Wadud, Jieun Yoo
- **University of Illinois Urbana-Champaign:** Mark Neubauer, David Jiang
- **University of Kansas:** Alice Bean



Backup

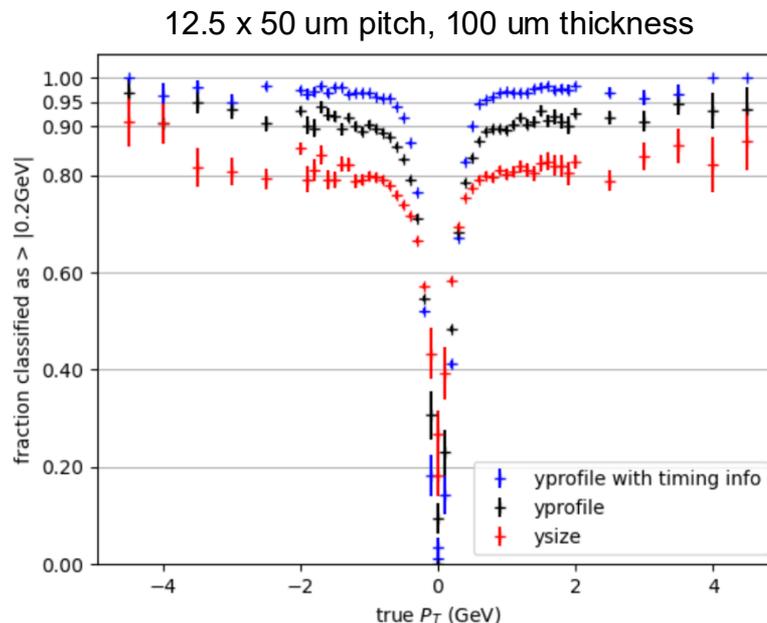
ML model: the p_T filter

- Trained with inputs:

1. Projected cluster size only.
Minimal information

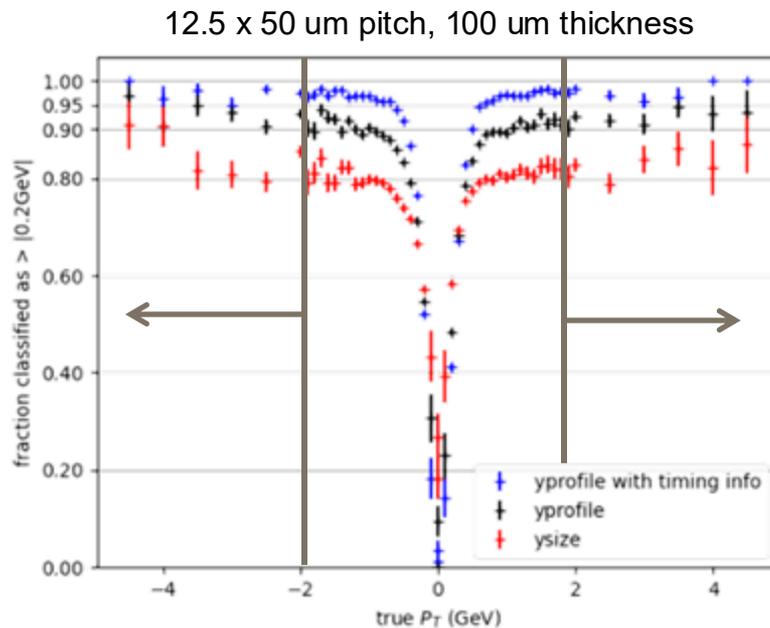
2. Projected cluster shape integrated over 4ns (selected for implementation)

3. Projected cluster shape at 8 200ps time points. 5-10% gain in signal efficiency



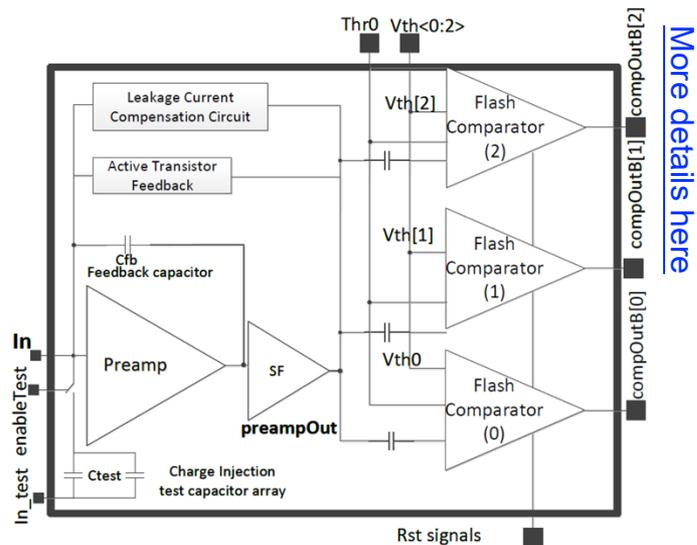
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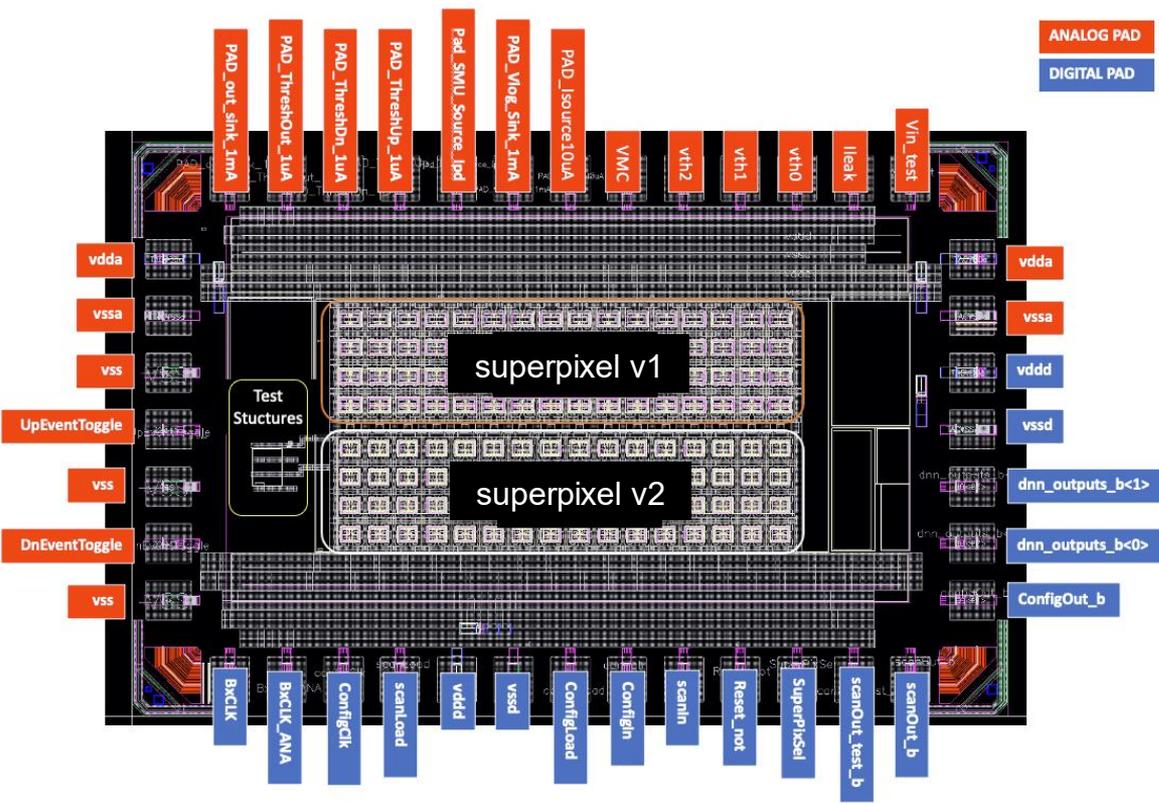


Implementation on-chip

- **Digitization** of the input
 - A 2-bit ADC assigns integrated charge to one of four bins: $[0, 400, 1600, 2400, \infty] e^-$
- **Minimal parameters** and **limited precision** per parameter
 - Storing these requires area on the ASIC

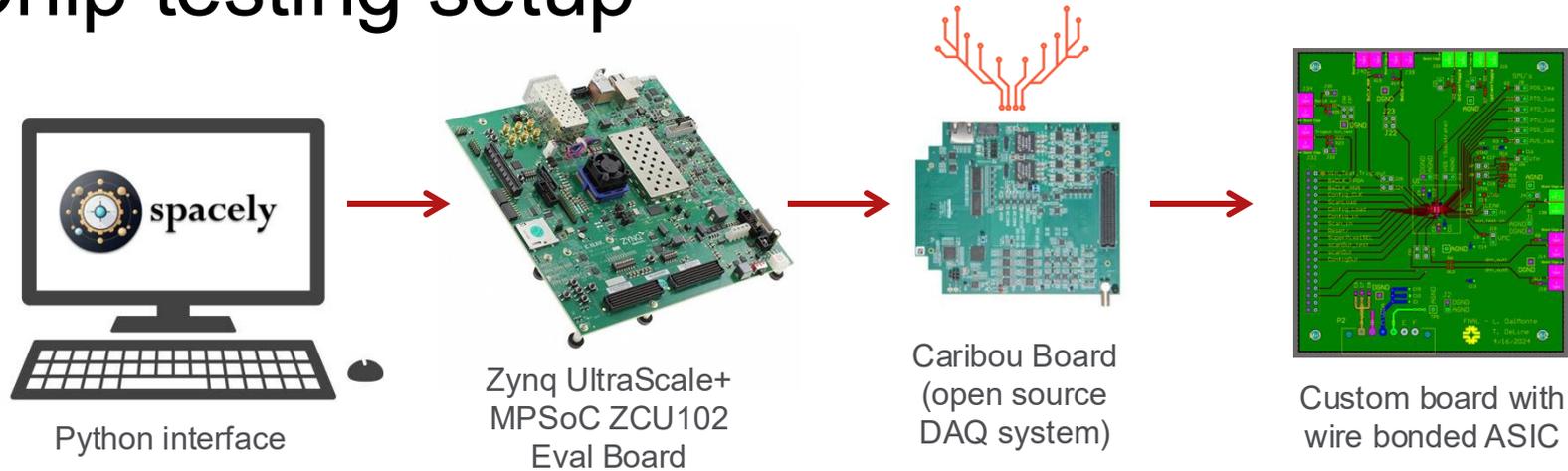


The chip



- Two copies of the digital p_T filter algorithm
- Superpixel v1 and v2 contain different versions of the analog front end

Chip testing setup



- Testing is underway at Fermilab, test stand being built now at Cornell
- Measurement plans include:
 - Noise and threshold dispersion, power usage, DNN performance

Spiking neural networks

- Convert waveform in each pixel to 2 **spike trains**
 - Train 1: spike when charge rises by 400 e-
 - Train 2: spike when charge falls by 400 e-
- **Low power**, but encodes time evolution of the current pulse
 - Spike trains as input to network
- First simple p_T filter has > 90% signal efficiency ([2307.11242](https://arxiv.org/abs/2307.11242))

