Qpixlar daq status

highlights

- Qpix reg control fully software controllable in pyqt
- Resets from LTC chip fully functional
  - Able to software control mask / enable / LTC shutdown per pin
- Tentative output data file format in an hdf5 file format
- Reset information stored along side 64 bit timestamp and metadata
  - Metadata to include FPGA number / IP for fine-tining which channel caused a reset in the qpixlar system, etc

Questions on ASIC control

- Where can I find documentation about what these bits do in the ASIC register?
- Updating any of these checkboxes automatically loads / configures ASIC registers
- Removes need of excel file / magic numbers
- What should these values be?