Kalindi Gosine

Spring 2025 Updates

January 24, 2025

Updates

- Finished testing DACs on HFA array with I2C driver
- Starting testing power on Carrier Board that just came in
- Ship boards to Wellesley
- Reading for Mei’s project, using some space to think about new transistor size
- Spoke to Kevin about starting on some firmware/software for Z-turn
- Classes, loss and found my mav id, ect

Updated DAC Commands

2 addressing bytes

Specifies device (AD5339 Address)

0	0	0	1	1	0	(X)	\

7 bit device address unique to AD5339
X set by A0 pin

read/write bit
R=1
W=0

Specifies which of the 2 DACs on the device (pointer byte)

(*)	(*)	0	0	0	0	DACB	DACA

(*) don't care bits
DACB = 1 if following data is for DAC B
DACA = 1 if following data is for DAC A

U8 controls LVDS_CM has address 0001 100_ (0001 100= 0xc)

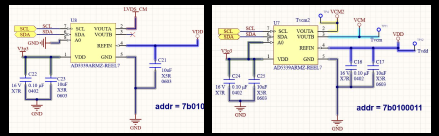
U7 controls VCM & VCM2 has address 0001 101_ (0001 101= 0xd)

LVDS_CM: DACB=0 DACA=1
00000001=0x01

VCM: DACB=1 DACA= 0
00000010=0x02

VCM2: DACB=0 DACA= 1
00000001=0x01

Update both VCM and VCM2:
00000011=0x03



2 data bytes

0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X

4 control bits
0010=0x2 for normal operation (last is 0 to update both DACs)

12 data bits

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal equivalent of the binary code, which is loaded to the DAC register
0 to 255 for AD5337 (8 bits)
0 to 1023 for AD5338 and AD5338-1 (10 bits)
0 to 4095 for AD5339 (12 bits)
N is the DAC resolution.

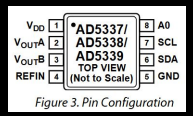


Figure 3. Pin Configuration

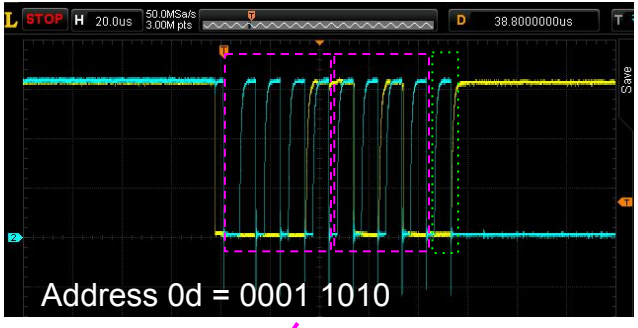
V_REF=VDD= 1.6V
N=12

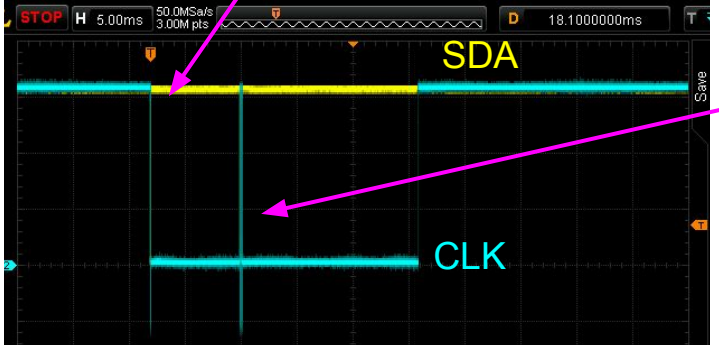
$$D = \frac{V_{OUT} \times 4096}{1.6V}$$

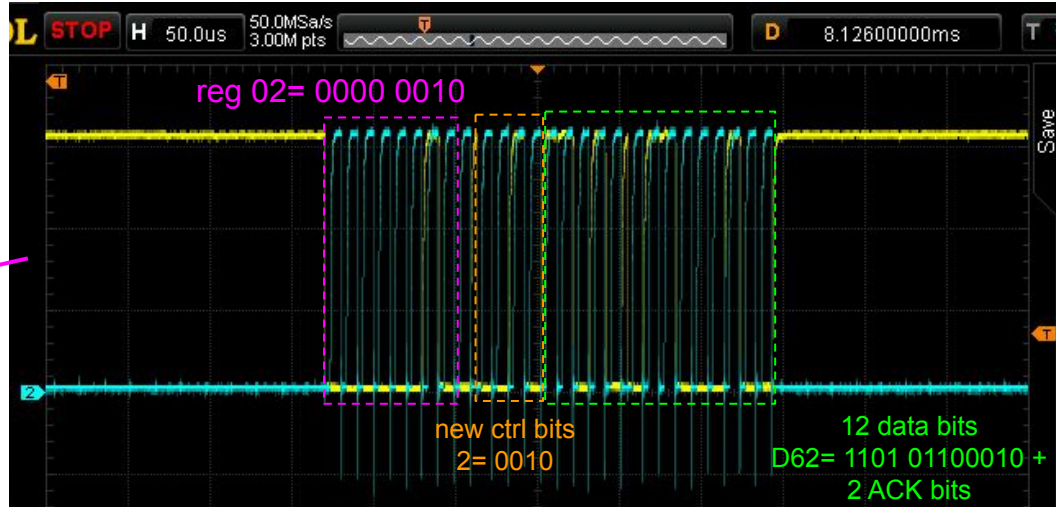
For Vout=1V
D=2560= 101000000000

0011 101000000000 = 0x3A00

Updated DAC Commands





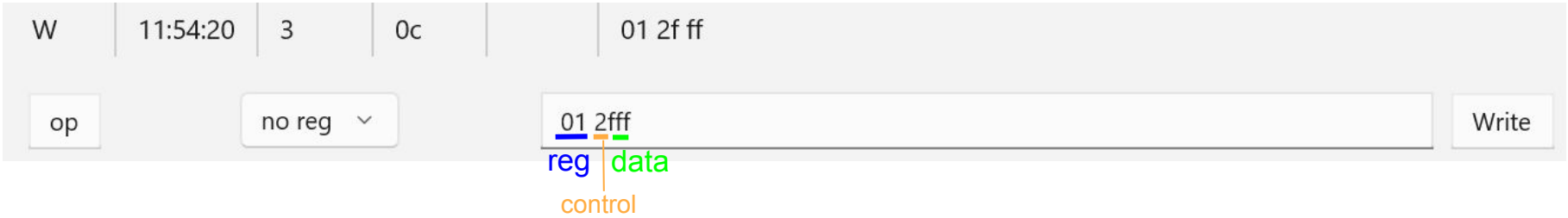


W	01:39:18	3	0d		02 2d 62

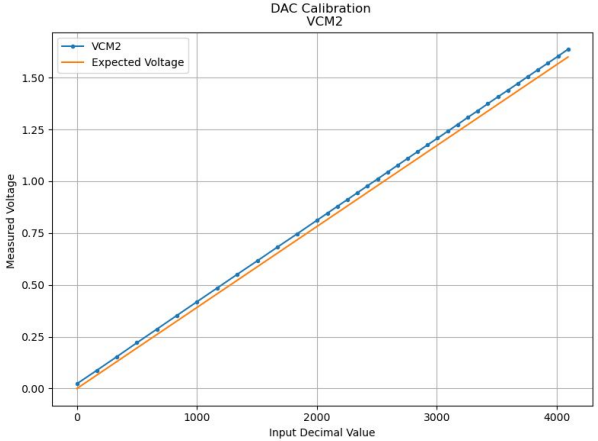
op | no reg | 02 2d 62 | Write

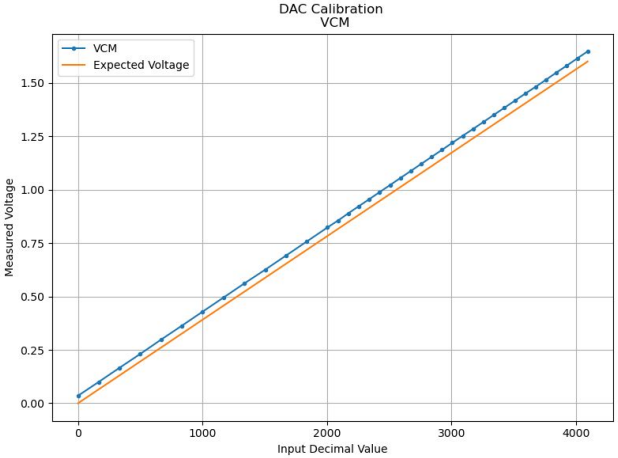
Voltages correctly set by I2C

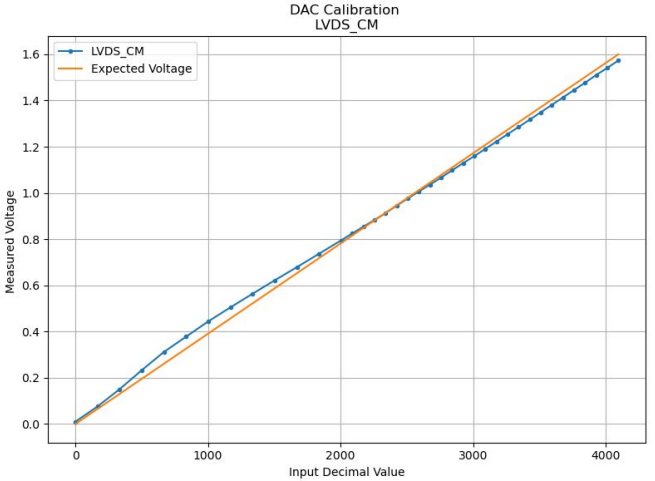
- The control bits must be set to 0010=0x2 (calls to update both registers on a chip after every command, even if only writing to one of them)
- Register can be written into data line ‘no reg’. 8 bit reg also works



DAC Calibration







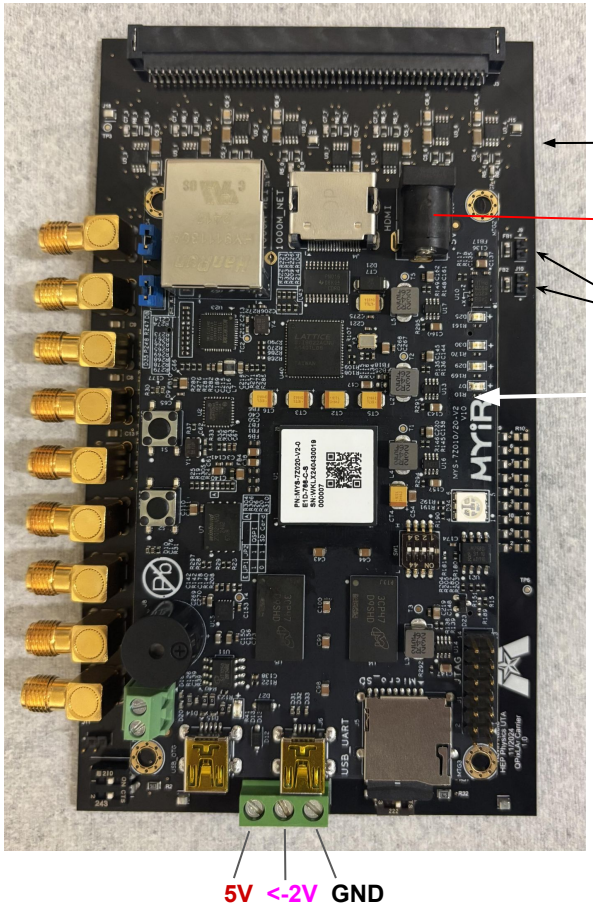
$$V_{expected} = \frac{D \times 1.6V}{4096}$$

Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:
D is the decimal equivalent of the binary code, which is loaded to the DAC register
0 to 255 for AD5337 (8 bits)
0 to 1023 for AD5338 and AD5338-1 (10 bits)
→ 0 to 4095 for AD5339 (12 bits)
N is the DAC resolution.

DAC Calibration 1_20_25.xlsx

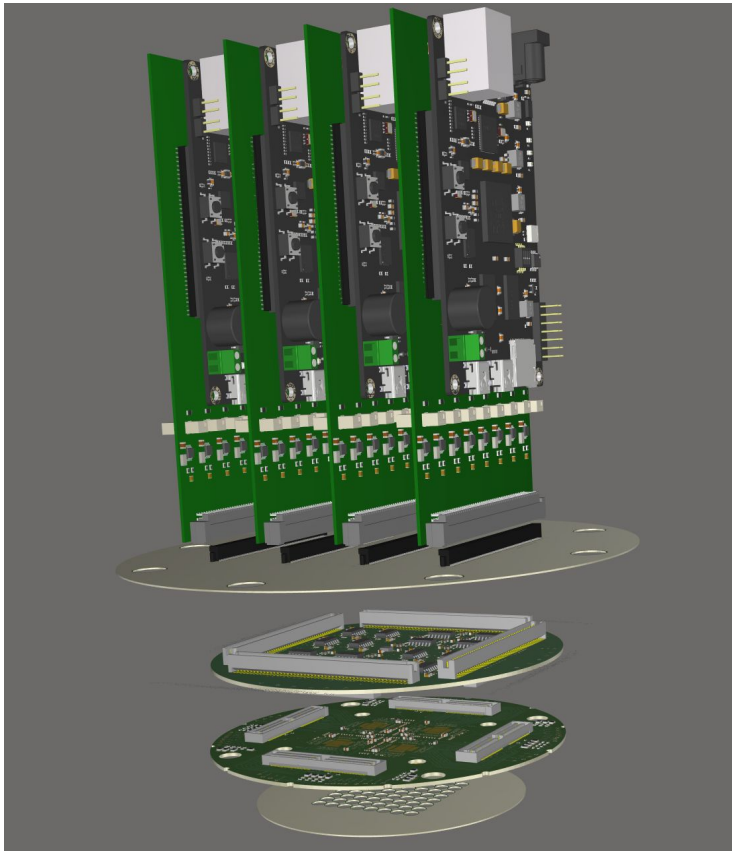


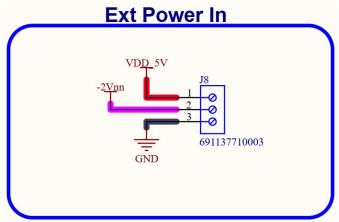
Carrier Board

or 5V to
Z-Turn

When connecting to HFA, short
each of these pairs to power

Mounted Z-Turn

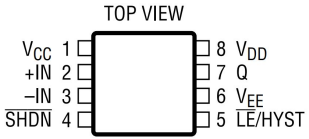




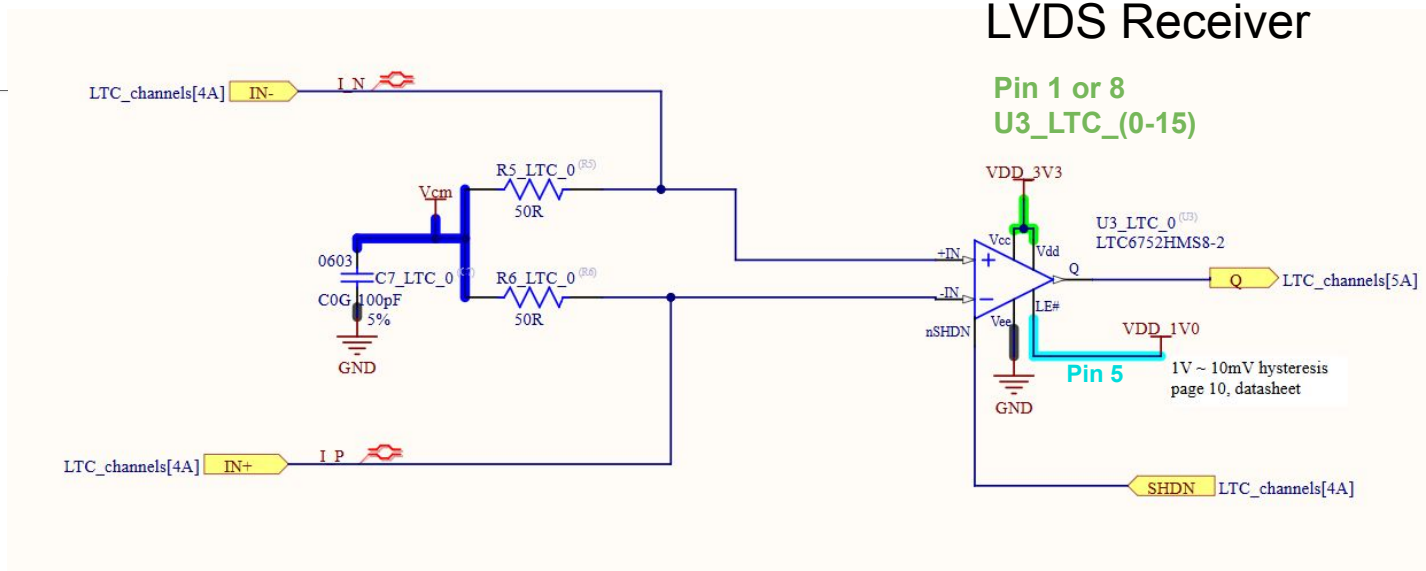
3.3V to LTC Chip

LTC6752-2

TOP VIEW



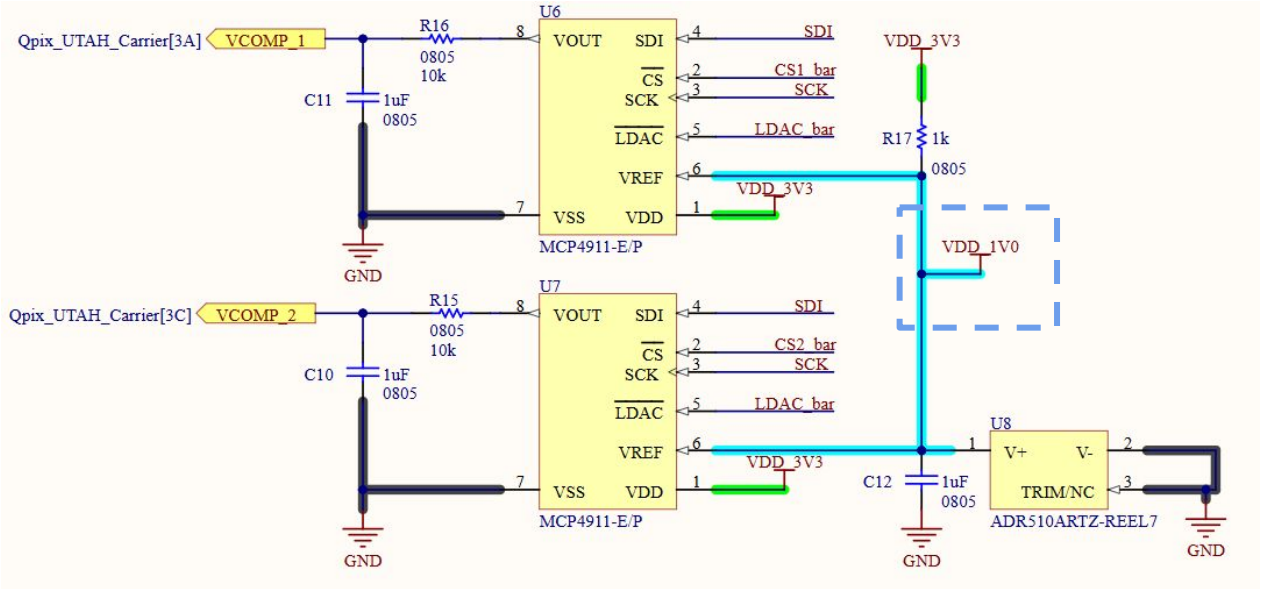
LVDS Receiver



LTC6752 LTC6752-1 LTC6752-2 LTC6752-3 LTC6752-4 - 280MHz, 2.9ns Comparator Family with Rail-to-Rail Inputs and CMOS Outputs

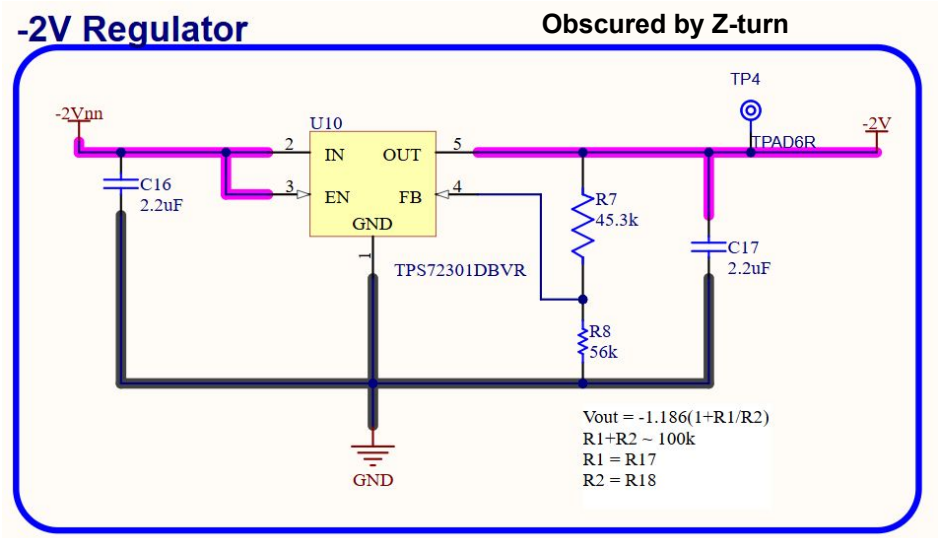
VDD_1V0

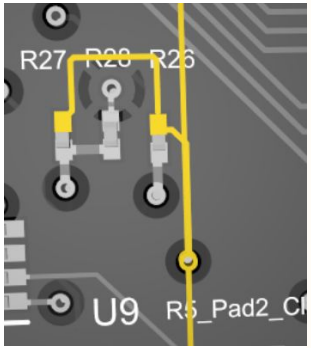
10 bit DACs

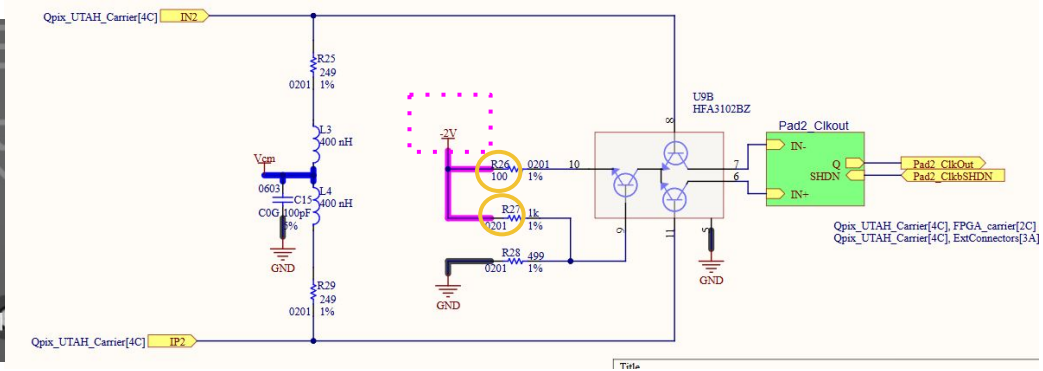


$$V_{OUT} = \frac{(V_{REF} \times D_n)}{2^n} \; G$$

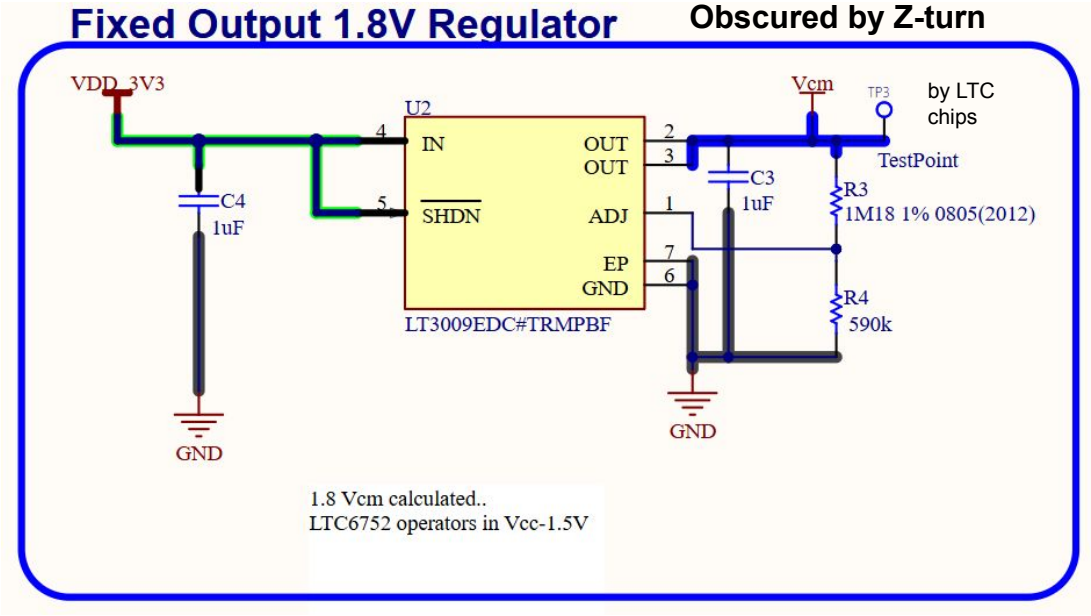
-2V

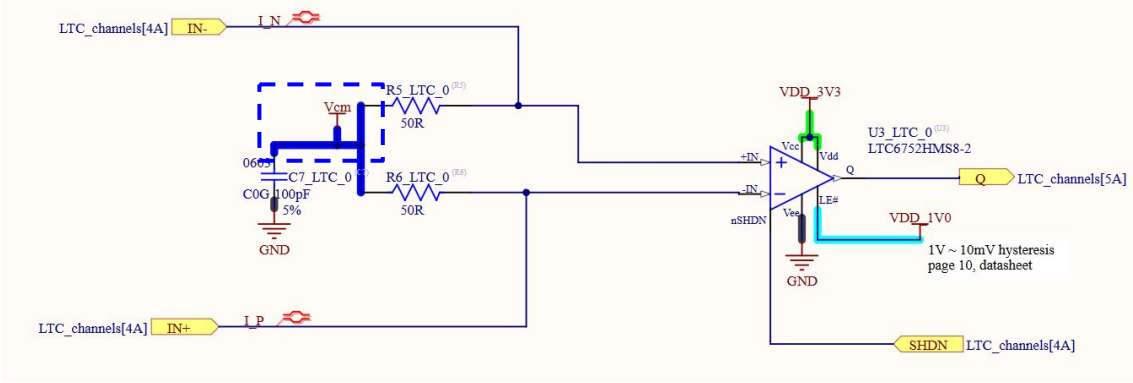

-2V Regulator
Obscured by Z-turn
TP4
-2Vnn
U10
IN
OUT
EN
FB
GND
TPS72301DBVR
TPAD6R
-2V
C16
2.2uF
R7
45.3k
C17
2.2uF
R8
56k
GND
Vout = -1.186(1+R1/R2)
R1+R2 ~ 100k
R1 = R17
R2 = R18


R27
R26
U9


Qpix_UTAH_Carrier[4C]
IN2
R25
249
0201
1%
L3
400 nH
Vcm
0603
C15
C0G 100pF
L4
400 nH
GND
R29
249
0201
1%
Qpix_UTAH_Carrier[4C]
IP2
-2V
R26
100
0201
1%
R27
1k
0201
1%
R28
499
0201
1%
GND
U9B
HFA3102BZ
Pad2_Clkout
IN-
IN+
Q
SHDN
Pad2_ClkOut
Pad2_ClkbSHDN
Qpix_UTAH_Carrier[4C], FPGA_carrier[2C]
Qpix_UTAH_Carrier[4C], ExtConnectors[3A]

VCM


Fixed Output 1.8V Regulator
Obscured by Z-turn
VDD_3V3
U2
IN
SHDN
OUT
OUT
ADJ
EP
GND
LT3009EDC#TRMPBF
C4
1uF
C3
1uF
Vcm
TP3
TestPoint
by LTC chips
R3
1M18 1% 0805(2012)
R4
590k
GND
GND
1.8 Vcm calculated..
LTC6752 operators in Vcc-1.5V


LTC_channels[4A]
IN-
L_N
Vcm
R5_LTC_0
50R
0603
C7_LTC_0
C0G 100pF
5%
R6_LTC_0
50R
GND
LTC_channels[4A]
IN+
L_P
VDD_3V3
U3_LTC_0
LTC6752HMS8-2
+IN
-IN
nSHDN
Vcc
Vdd
Vee
LE#
Q
LTC_channels[5A]
VDD_1V0
1V ~ 10mV hysteresis
page 10, datasheet
GND
SHDN
LTC_channels[4A]

January 31, 2025

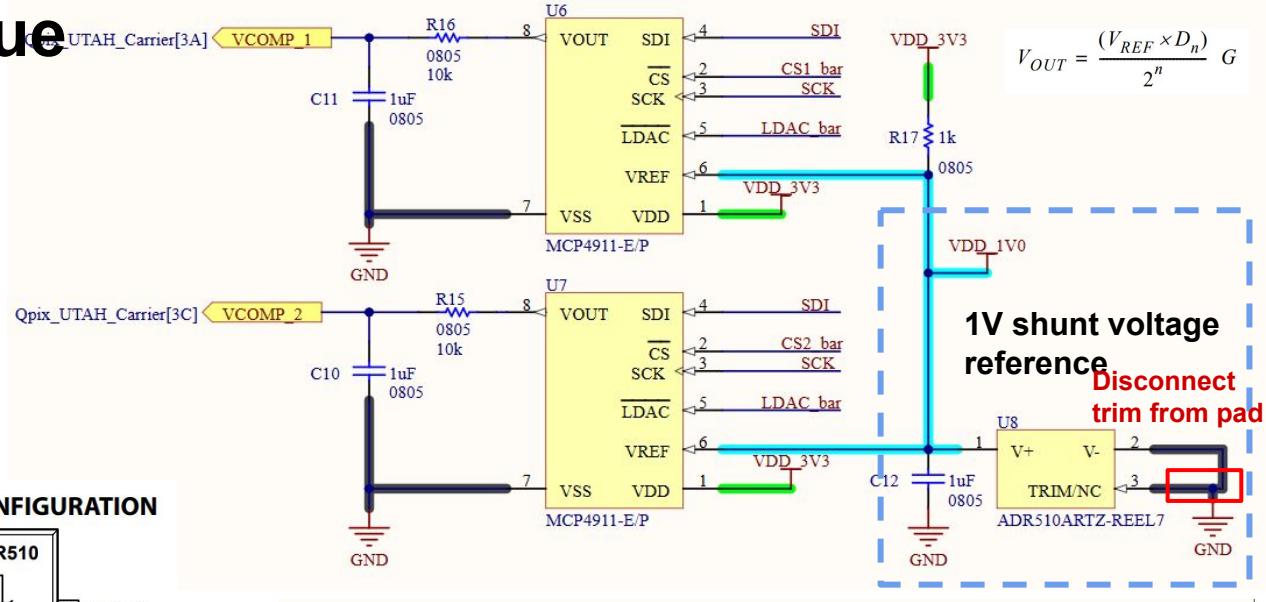
Updates

- Power up voltages on the carrier board all work
  - 3.3V, VDD_1V0, -2V, VCM
  - Had one issue with the VDD_1V0 that was resolved
  - Confirmed on all of the carrier boards
- Currently working on connecting they carrier board to HFA board with 100 pin ribbon cable and checking power up voltages on these

The VDD_1V0 Issue

VDD_1V0= 1.00V

Pin 3 on shunt voltage reference must be disconnected from pad (desoldered, kapton tape, resolder pins 1&2)



$$V_{OUT} = \frac{(V_{REF} \times D_n)}{2^n} G$$

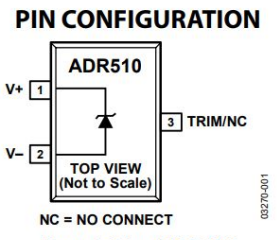
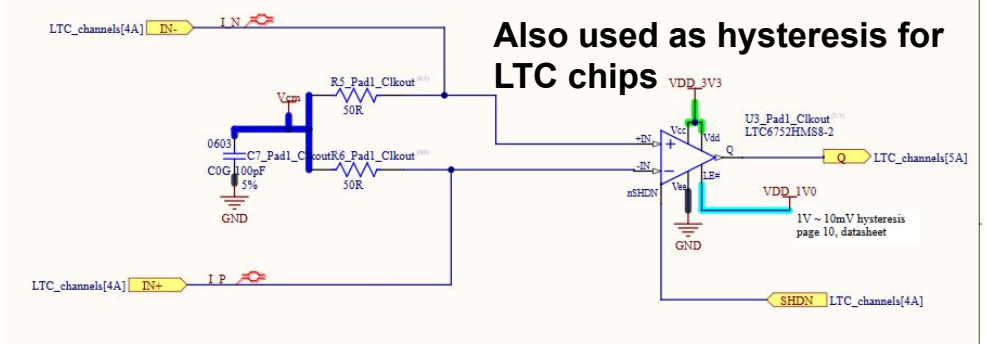


Figure 1. 3-Lead SOT-23-3

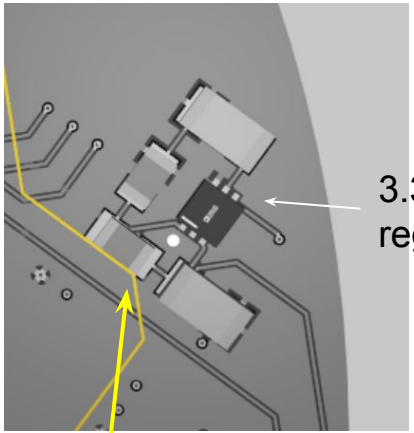


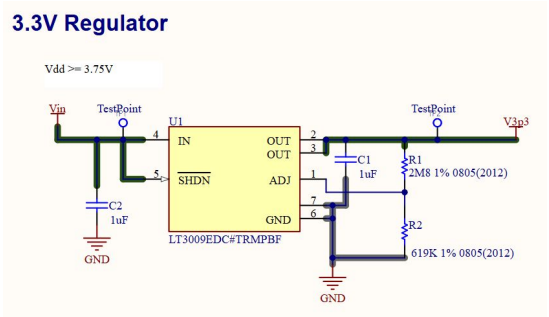
[ADR510 | 1.0 V Precision Low Noise Shunt Voltage Reference | Data Sheets]

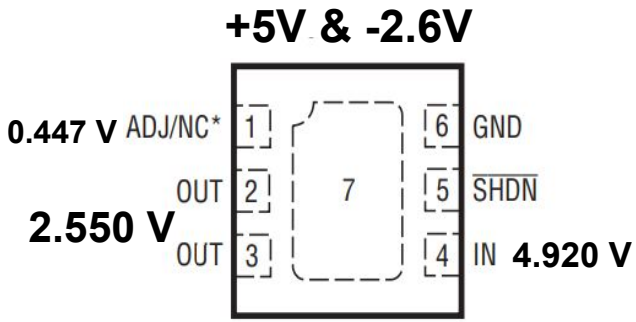
February 7, 2025

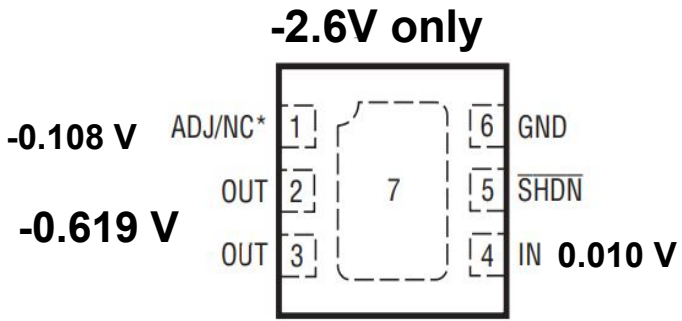
Troubleshooting V3p3

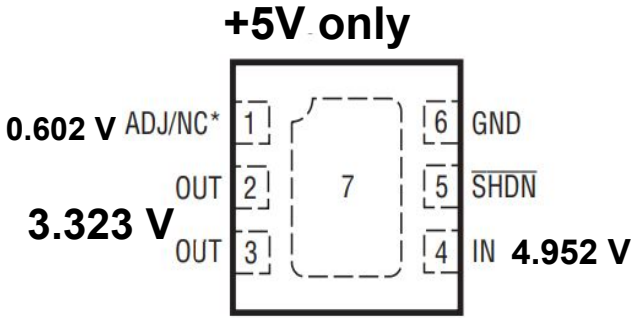
According to [3.3V regulator datasheet], the output should be 3.3V based on the resistor combination and the ADJ pin should be maintained at 600mV.







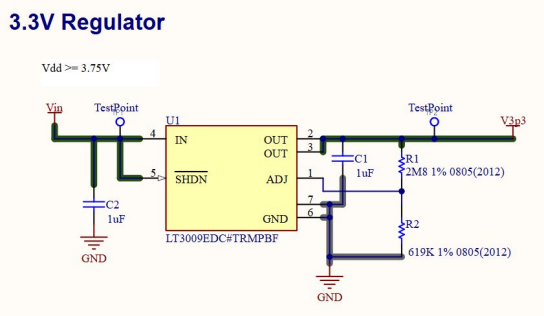




Troubleshooting V3p3

Confirmed R1 and R2 values are correct

Powered with only +5V and measured 3.324V pin3 and 0.602V at pin1



Finite resistance between -2Vnn and V3p3 (only -2Vnn powering board):

$$I_{R1} = \frac{V3p3 - V_{ADJ}}{2.8M\Omega} = \frac{-0.612 + 0.108}{2.8M\Omega} = -0.18\mu A$$

$$-2Vnn - IR = V3p3$$

$$(-2.6V) - (-0.18\mu A)R = -0.612V$$

$$R = 11M\Omega$$

Confirmed the stagnant voltage on V3p3 when only -2Vnn is ON varies linearly with the value of -2Vnn

(-2Vnn=-2.6V, V3p3= -0.619 → -2Vnn= -1.8V, V3p3 = -0.500 V)

No resistor between 8-13MegOhms on Altium for HFA board. Unclear where this is coming from and why these points are not completely isolated

Next

- Solder the missing R10 resistors (probably tuesday)
- Talk to someone about what the plan is for this connection between -2Vnn and V3p3 that should not exist
- Send analog board to Penn (?) for them to send w chips for wirebonding

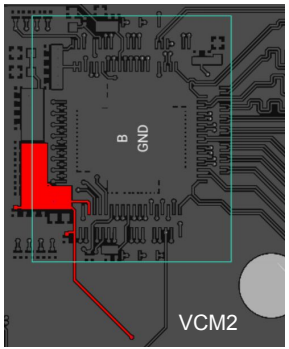
February 14, 2025

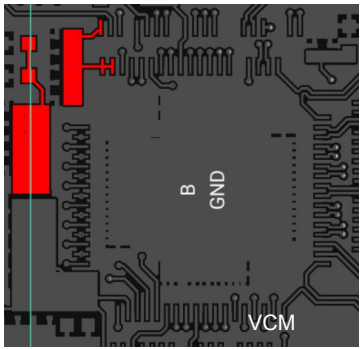
Updates

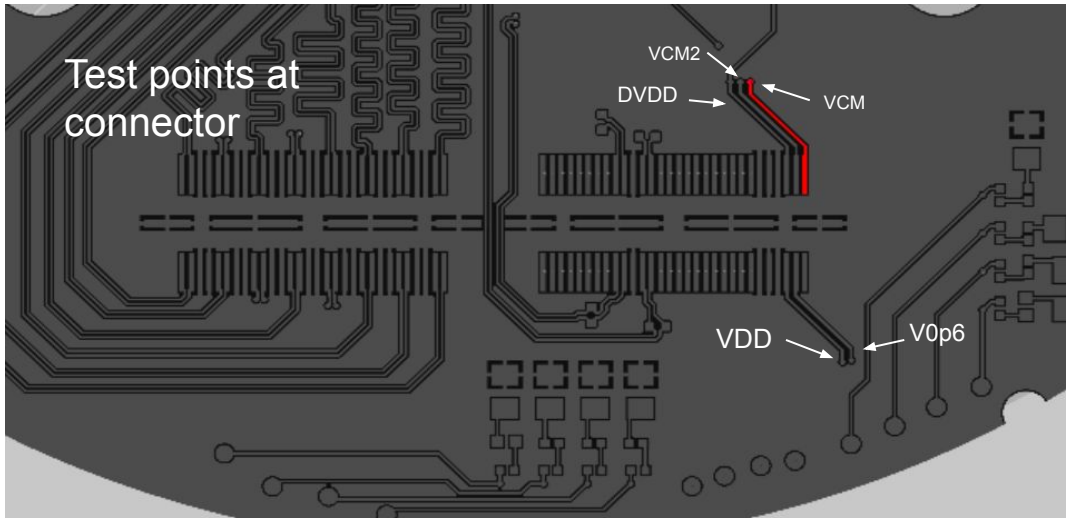
- Analog board testing
- Shipped board to FNL for wire bonding
- Stuffed missing components onto Carrier boards for ASIC slow control

Confirmed ASIC voltages not connected to ground

They are isolated from the board ground and test points near connector are connected to pads at ASIC

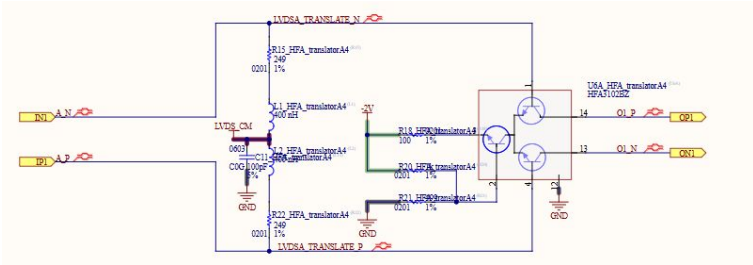






For a single ASIC board when connected to HFA, all ASIC voltages are shorted to ground

- When not connected to HFA, ASIC voltages are all isolated from board ground
- When connected to HFA, ASIC voltage test points on HFA are shorted to ground
- When HFA is powered from Carrier Board, ASIC voltage test points are correct
- When HFA is powered from Carrier Board and connected to ASIC board, all voltage test points are shorted to ground
- No issue with the other two ASIC boards with either of our 2 HFA boards
  - Confirmed diff pairs on HFA chips have correct resistances between them



Next

- Waiting to get boards back from wire bonding
- Checking connections once the mini-feedthrough and analog mounting boards come in
- Talking to labs for HEPIC summer internship this week

March 7, 2025

Wire Bonded ASICs came back

Confirmed ASIC voltages (Vdd, dVdd, V0p6) on HFA board when connected to ASIC board (with 1 bonded chip) and powered (only 5V through Carrier board)

These test points were properly isolated from each other and GND

Set up test bench

Issue: Z-turn connected to Carrier board is emitting a loud high pitched noise when the board is powered with more than 0.1Amps (needs 0.6Amp current to supply the 5V) which it was not doing previously.

Zturn+Carrier Issue

Previously, 56mA was needed to power the zturn through the carrier to 5V. Now, it only requires 23mA and is emitting a very loud noise from the buzzer of the zturn for currents greater than 10mA.

When the zturn is powered independently of the carrier board (via USB), there is no noise.

Writing to the SD card did not make any change.

Despite the beeping, voltages on the carrier board are correct (3.3V at LTC chip)

Issue persists across other zturns and carrier boards.

March 18, 2025

ZTurn Current Draw

Removed R121 (allowing current into buzzer)

Carrier board + Zturn 5V power Current draws:

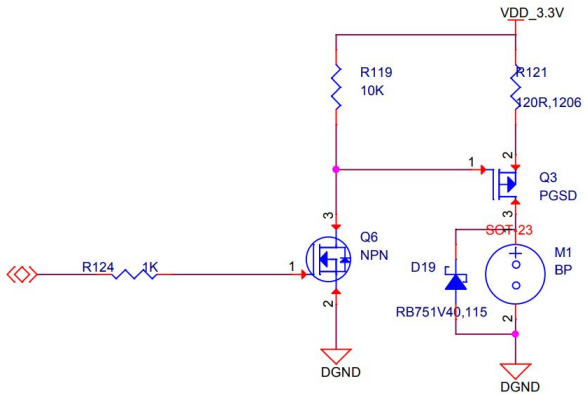
ONE: 0.22Amps(zturnI, with and without SD card)

0.60Amps (zturnII, with SD) 0.23Amps(zturnII, no SD)

TWO: 0.23Amps(zturnI, with and without SD)

0.47Amps(zturnII, with SD) 0.23Amps(zturnII, n

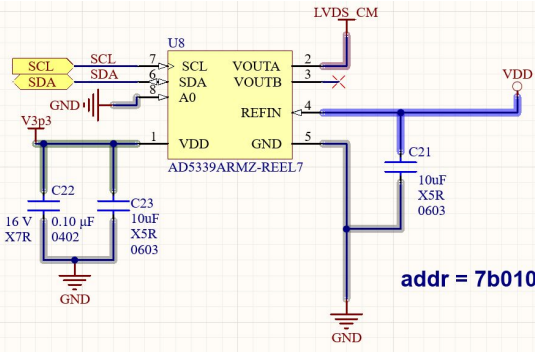
No buzzing



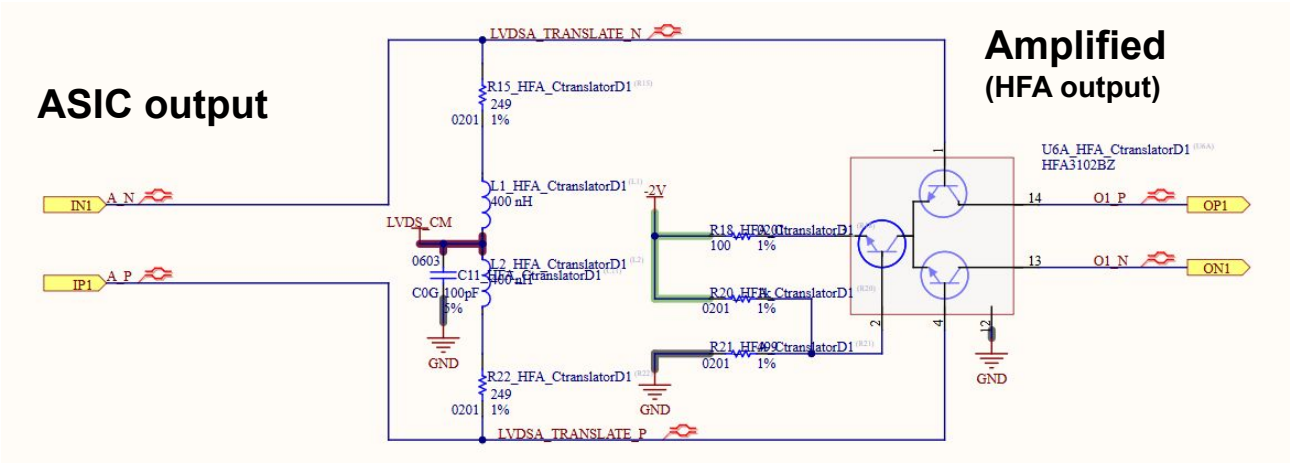
https://www.myirtech.com/download/Zynq7000/Z-TURNBOARD_schematic.pdf

April 4/11, 2025

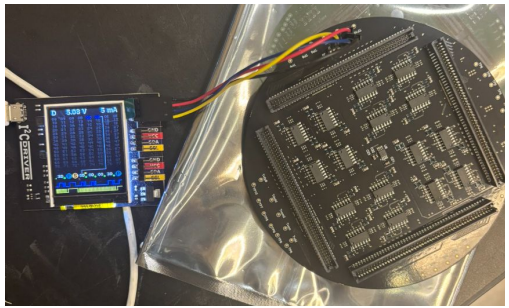
Regarding LVDS_CM Ringing



LVDVS_CM works only on the HFA board to control the amplification of the ASIC signal.

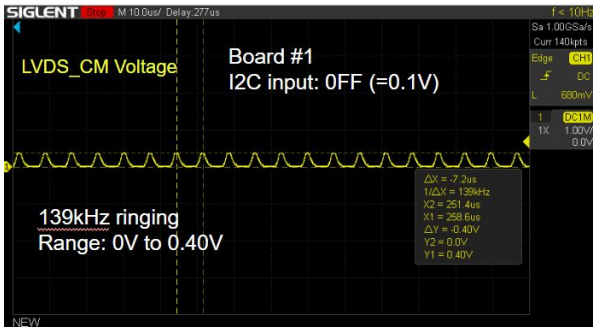


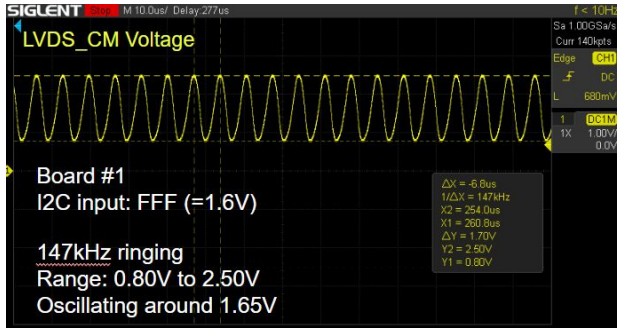
Re: LVDS_CM ringing, I2C Driver + HFA Test

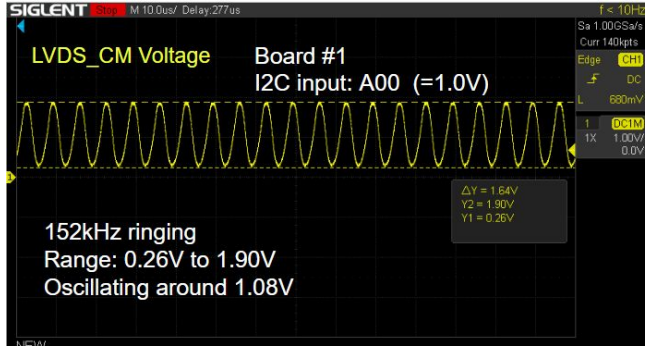


Repeated our previous test of just I2C driver and HFA board to see LVDS_CM control.

When we tested this in Jan/Feb, we saw LVDS_CM (and VCM1 and VCM2) voltages controlled well by the driver. The issue is that we tested using a multimeter, making us blind to the ringing which does time average to the correct voltage.

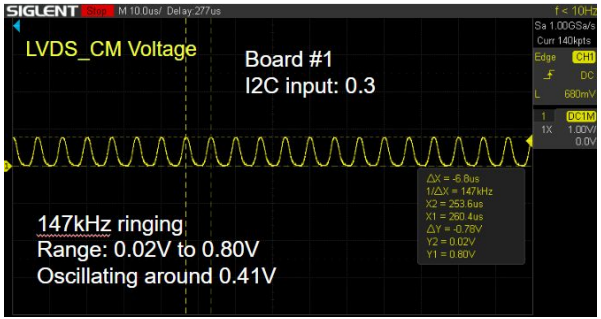


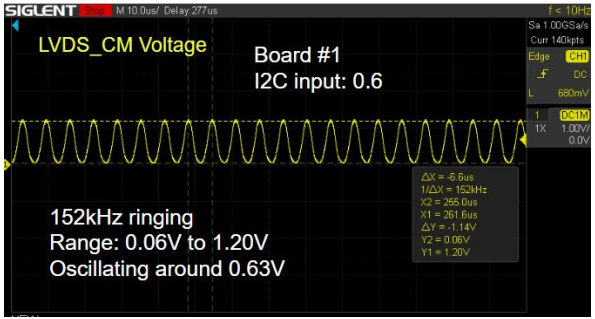


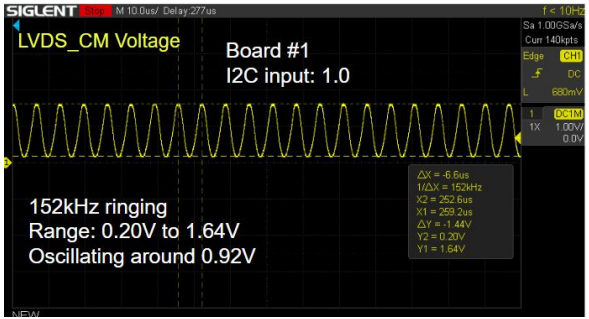


Re: LVDS_CM ringing, Carrier(+5V)+Zturn+HFA

Ringing is identical when controlled via carrier and zturn (only +5V) is supplied

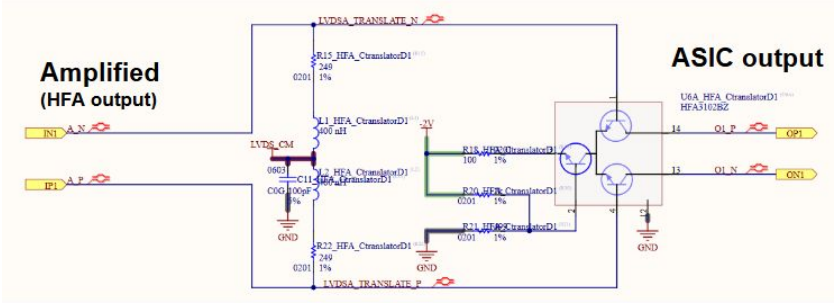


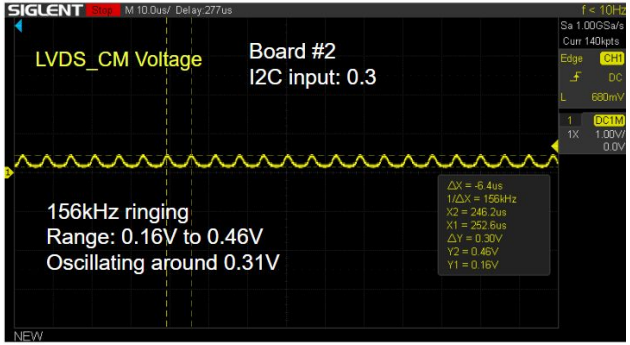


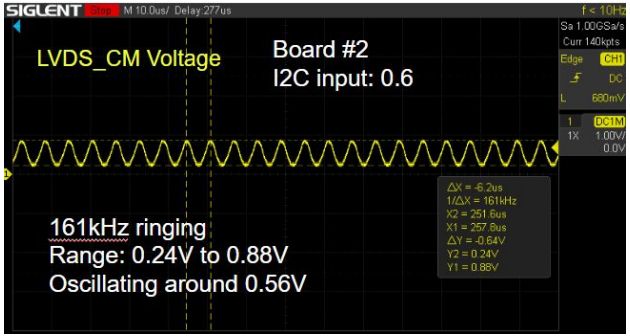


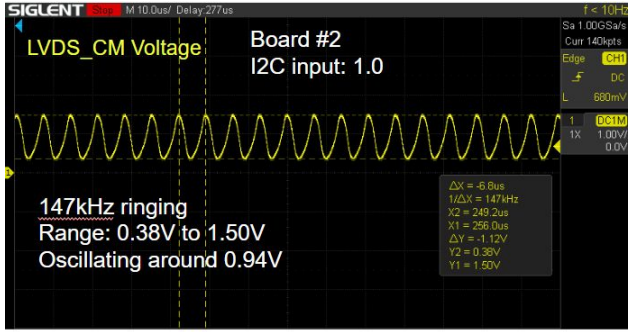
Carrier (+5V) + ZTurn + HFA + (Feedthrough & ASIC Mount) + 1 Chip ASIC Board

The idea was that maybe the HFA doesn't like its ASIC differential pair floating so connecting the ASIC would fix this.









The problem with the -2Vnn input

In all the preceding tests we only powered the Carrier board with +5V which is all that is needed for these I2C voltages. The -2V is necessary for the amplification by the HFAs.

Back in Jan/Feb that there was some connection (11MΩ) between the -2Vnn and V3p3 voltages on the HFA board which was reducing V3p3 from 3.3V to 2.7V.

When testing the 1 Carrier + HFA + 1 chip ASIC:

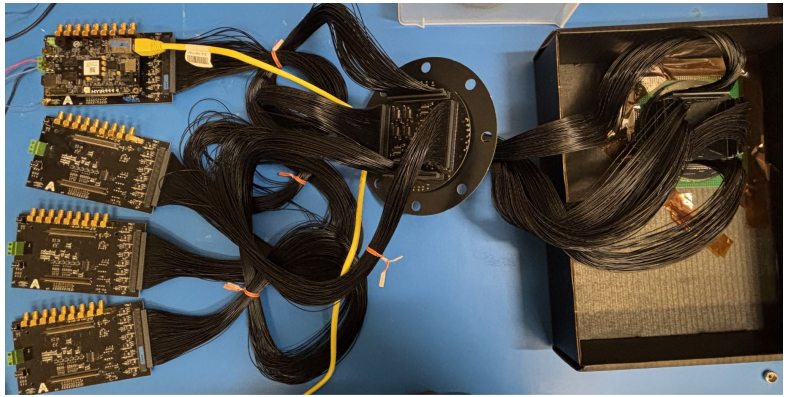
When we apply the -2.7V (2Vnn) through the carrier board we were seeing the V3p3 at the LVDS DAC reduced from 3.3V to 1.88V and the LVDS_CM voltage set to -0.88V and no longer controllable via I2C. dVdd was also reduced from 1.6V to 1.16V (problematic since this is a voltage which does go down to ASIC)

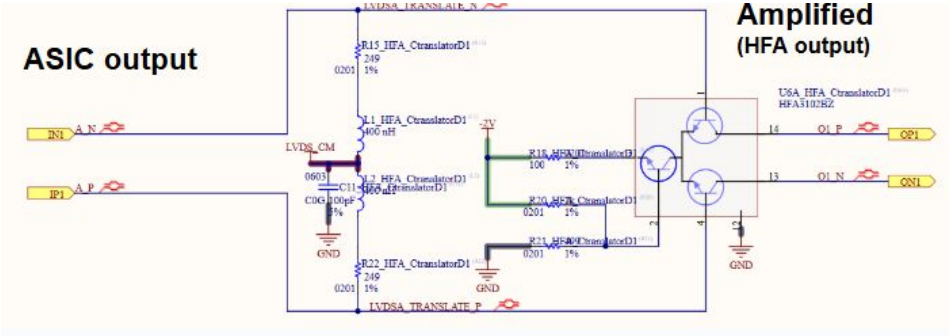
-2Vnn problem is solved by terminating all HFA differential pairs

Connecting all 4 carrier boards (even if three of them are unpowered) and the 4 chip ASIC board isolates the -2Vnn voltage from the rest of the board again.

V3p3 at the LVDS_CM DAC is again 3.3V. dVdd is again 1.6V.

In this configuration LVDS_CM is 0V and not controllable via I2C.





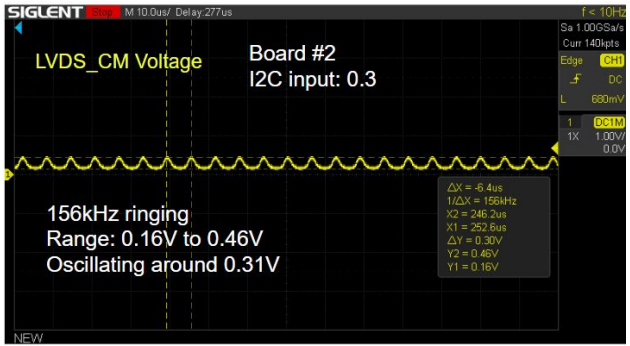
Powered up all Carrier Boards (+3 ZTurns)

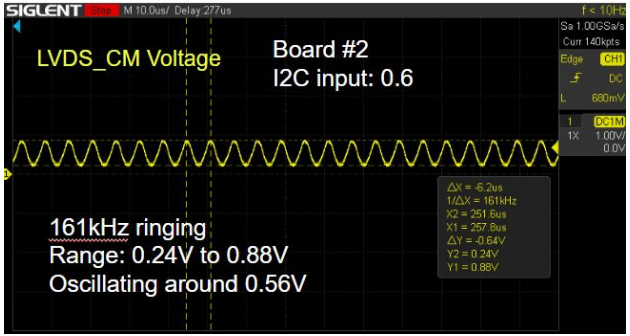
Set up is all good, just waiting on firmware for testing

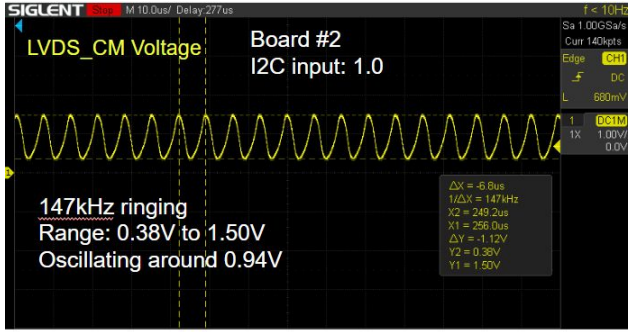
April 15, 2025
Kalindi Gosine UTA

Carrier (+5V) + ZTurn + HFA + (Feedthrough & ASIC Mount) + 1 Chip ASIC Board

The LVDS DAC had an unexplained ringing in its voltage output.
We see later that connecting all four carrier boards sets the voltage to undefined and it rests at 0V





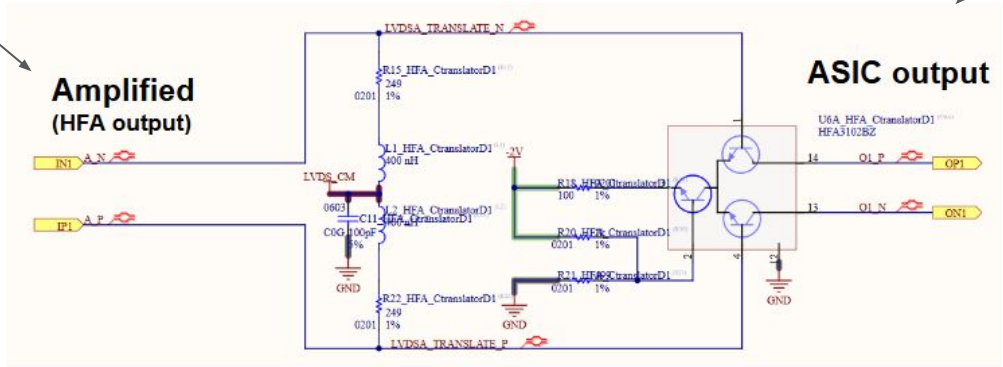


The diff pairs connected to the carrier boards need to be defined

Otherwise we were seeing connection between -2Vnn (-2.7V) and LVDS_CM, dVdd, and V3p3

All HFAs must be connected to carrier boards

These can be left unconnected

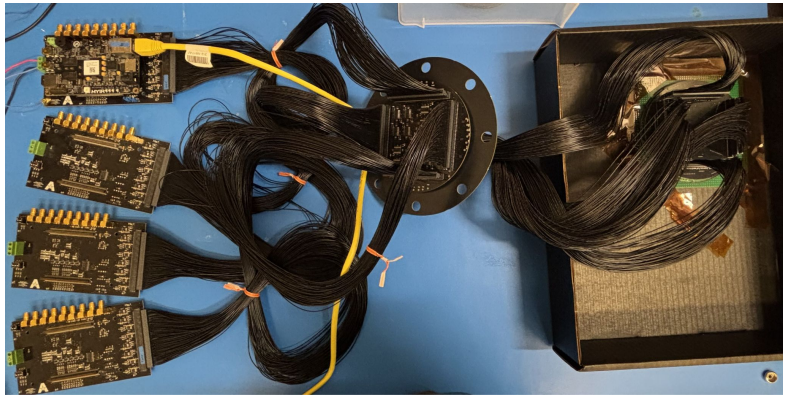


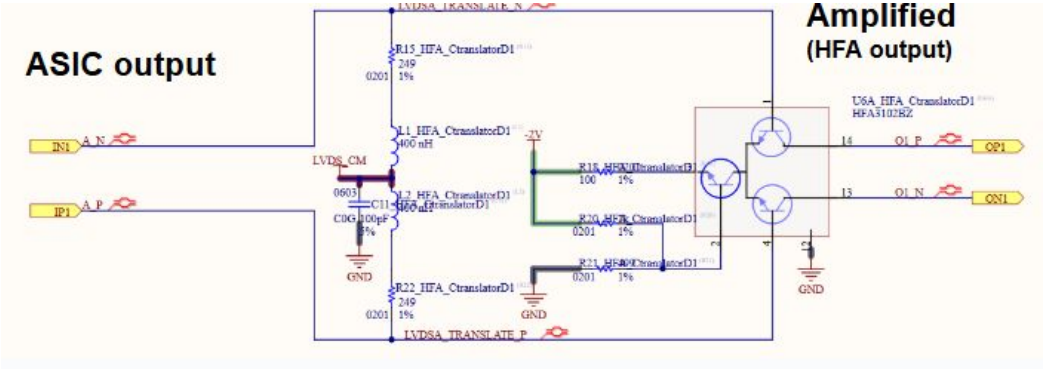
-2Vnn connection problem is solved by terminating all HFA differential pairs

Connecting all 4 carrier boards (even if three of them are unpowered) and the 4 chip ASIC board isolates the -2Vnn voltage from the rest of the board again.

V3p3 at the LVDS_CM DAC is again 3.3V. dVdd is again 1.6V.

In this configuration LVDS_CM is 0V (but isolated from ground) and not controllable via I2C.





Implications

LVDS_CM:

- Although LVDS_CM=0V, it can be set by an external power supply (i.e. we could adjust it by applying a voltage on a wire from the power supply)
- It looks like this will have to be the case, connecting a wire to some LVDS_CM point on the board and controlling the voltage from the supply.

Both 1 chip and 4 chip boards are usable

Meeting Notes

Go ahead with no LVDS_CM, could still work. The ASIC should pull up to 2V. Then check LVDS voltage on the plane. Ideally it would have been 0.8V.