
# Chip Design for Gravitational Wave Detectors

Alberto Gatti, Ciana Barretto and Filip Tavernier

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# Introduction


- Integrated circuit and sensor design
- Two currently active projects for GW detectors:
  - Einsten Telescope (ET)
  - Laser Interferometer Space Antenna (LISA)
- Supervisor: Prof. Dr. Ir. Filip Tavernier



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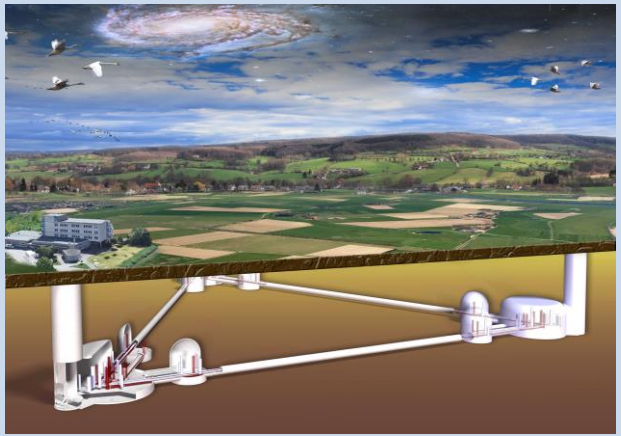
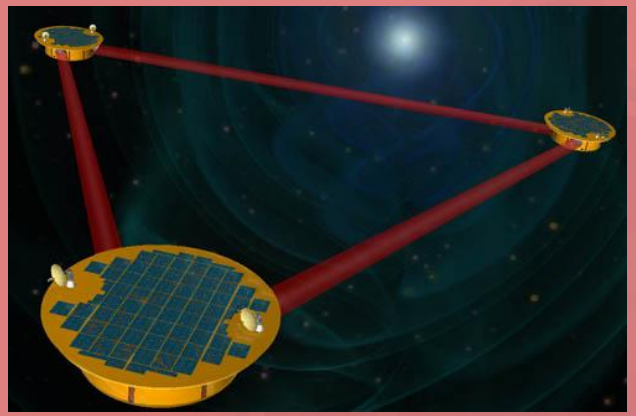
# Two Different Design Cases

**Cryo-CMOS circuits for ET cryogenic chambers**



Deep-cryogenic environment

**Optical Front End Electronics for LISA**



Radiation exposure



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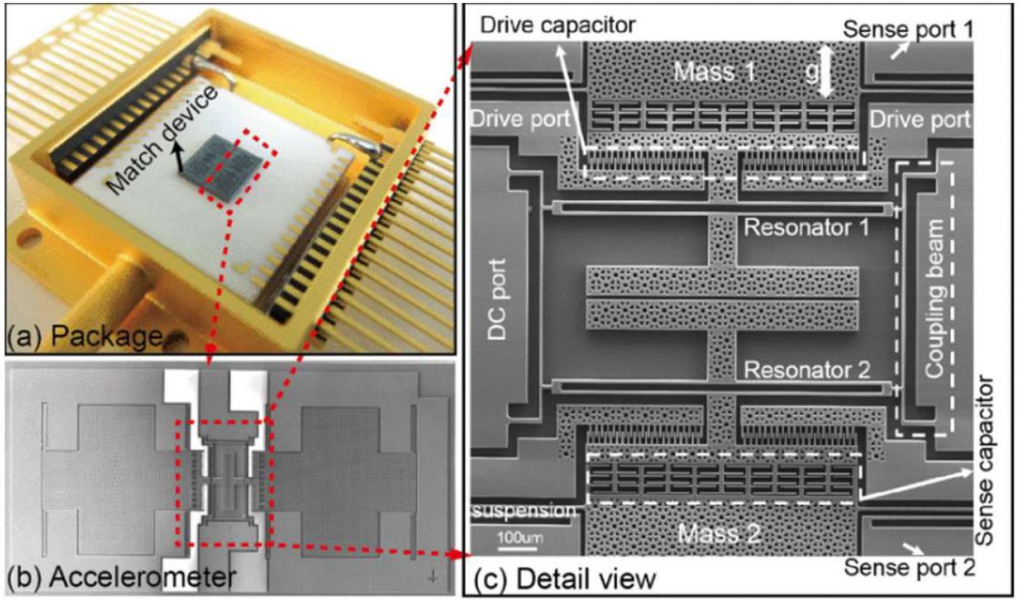
# Cryo-CMOS and sensors for ET




- Application: ultra-cold vibration control for the interferometer mirrors
- MEMS accelerometers with novel cryogenic CMOS signal conditioning integrated circuits



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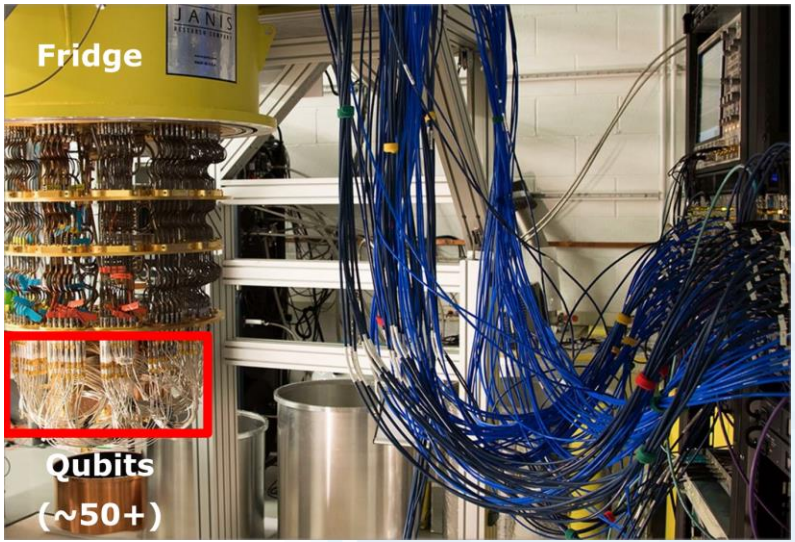
# Why Custom Integrated Circuits?

- Main advantages:
  - ☺ Tailored for the application
  - ☺ VLSI integration
    - ☺ Less volume and cabling
  - ☺ Less power
  - ☺ Signal integrity
    - ☺ Amplification/conditioning close to sensor
- Specific challenges:
  - ☹ Extreme environments
  - ☹ **Device modeling**




[J. C. Bardin et al., ISSCC 2019]



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# Compact Models for Circuit Simulation

- Compact model ≠ TCAD model!
  - TCAD models are not fast enough
- Compact models try to capture the electrical behavior of the device
  - Generally **not** derived from the underlying physics
- *Model cards* = set of device parameters

```
**********
* BSIM4.5.0 model card for p-type devices
**********
.model  pch_svt.1 pmos  ( level = 54
**********
*                  MODEL FLAG PARAMETERS
**********
+lmin = 2.59e-008      lmax = 2.51e-007     wmin = 'wmin_p_svt'
+wmax = 'wmax_p_svt'   version = 4.5        binunit = 1
+paramchk = 1          mobmod = 1           capmod = 2
+igcmod = 2            igbmod = 1           geomod = 0
+diomod = 1            rdsmod = 0           rbodymod= 0
+rgeomod = 0           rgatemod= 0          permod = 1
+acnqsmod= 0           trnqsmod= 0
**********
*               GENERAL MODEL PARAMETERS
**********
+tnom = 25             toxe = 'toxp_svt'    toxp = 1.012e-009
+toxm = 'toxp_svt'     dtox = 2.5e-010      epsrox = 3.9
+toxref = 1.2e-009     wmlt = 1             wint = 0
+lint = 4.1628e-011    ll = 0               wl = 0
+lln = 1               wln = 1              lw = 0
+ww = 0                lwn = 1              wwn = 1
+lwl = 0               wwl = 0              xl = '0+dxlp_svt'
+xw = '0+dxwp_svt'     dlc = 2.6887e-009    dwc = 0
+xpart = 0
**********
*                        DC PARAMETERS
**********
+vth0 = '-0.46149+dvthp_svt+sdvtp_svt+sigvtp_svt'  k1 = 0.35256
+lk1 = -0.0024567      k2 = 0.017398        k3 = 0.27044
+k3b = 0.07434         w0 = 1e-007          dvt0 = 0.52272
+dvt1 = 0.50091        dvt2 = -0.021065     dvt0w = 0.013
+dvt1w = 5984800       dvt2w = 0.05         dsub = 4.1202
```



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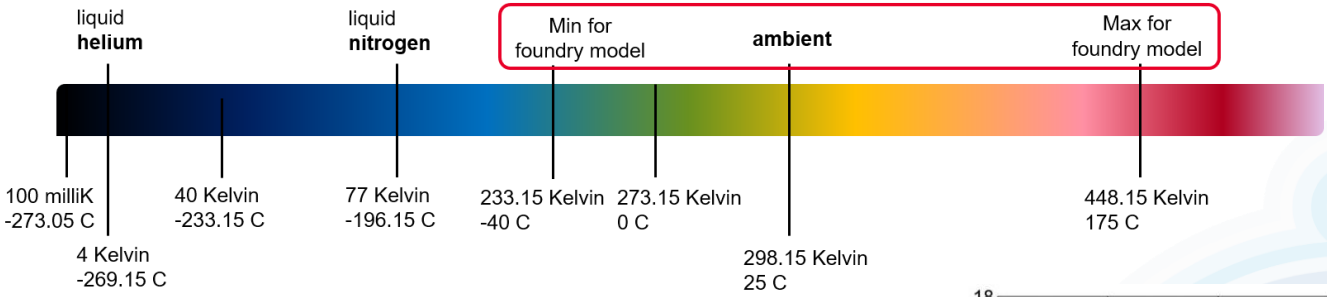
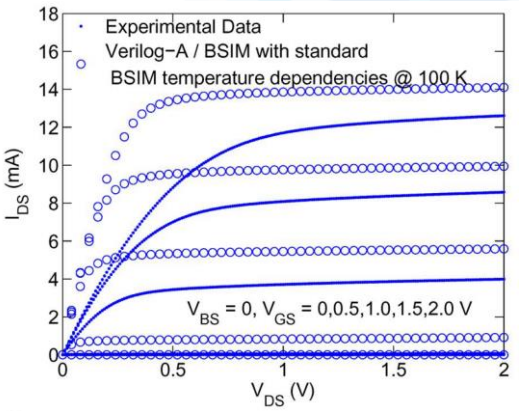
# Deep-cryogenic device modeling for ET




- ☹ Compact models provided by foundries are unable to describe cryogenic behavior
  - ☹ Cryogenic characterization and modeling are required
- ☺ T is very well regulated




[A. Akturk et al., Trans. El. Dev., 2010]



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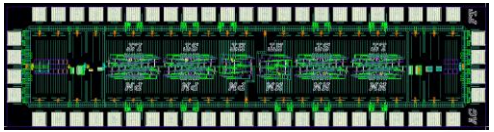
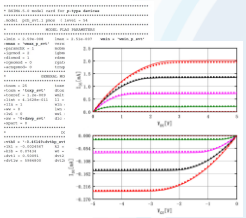
# Cryo-CMOS Design Roadmap

Design of test structures in different nanoscale CMOS technologies (supplied by foundries)



Characterization inside a cryostat and model parameter extraction

Editing of foundry models to enable cryogenic Integrated Circuit simulation



Design of cryogenic Application Specific Integrated Circuits (ASICs)



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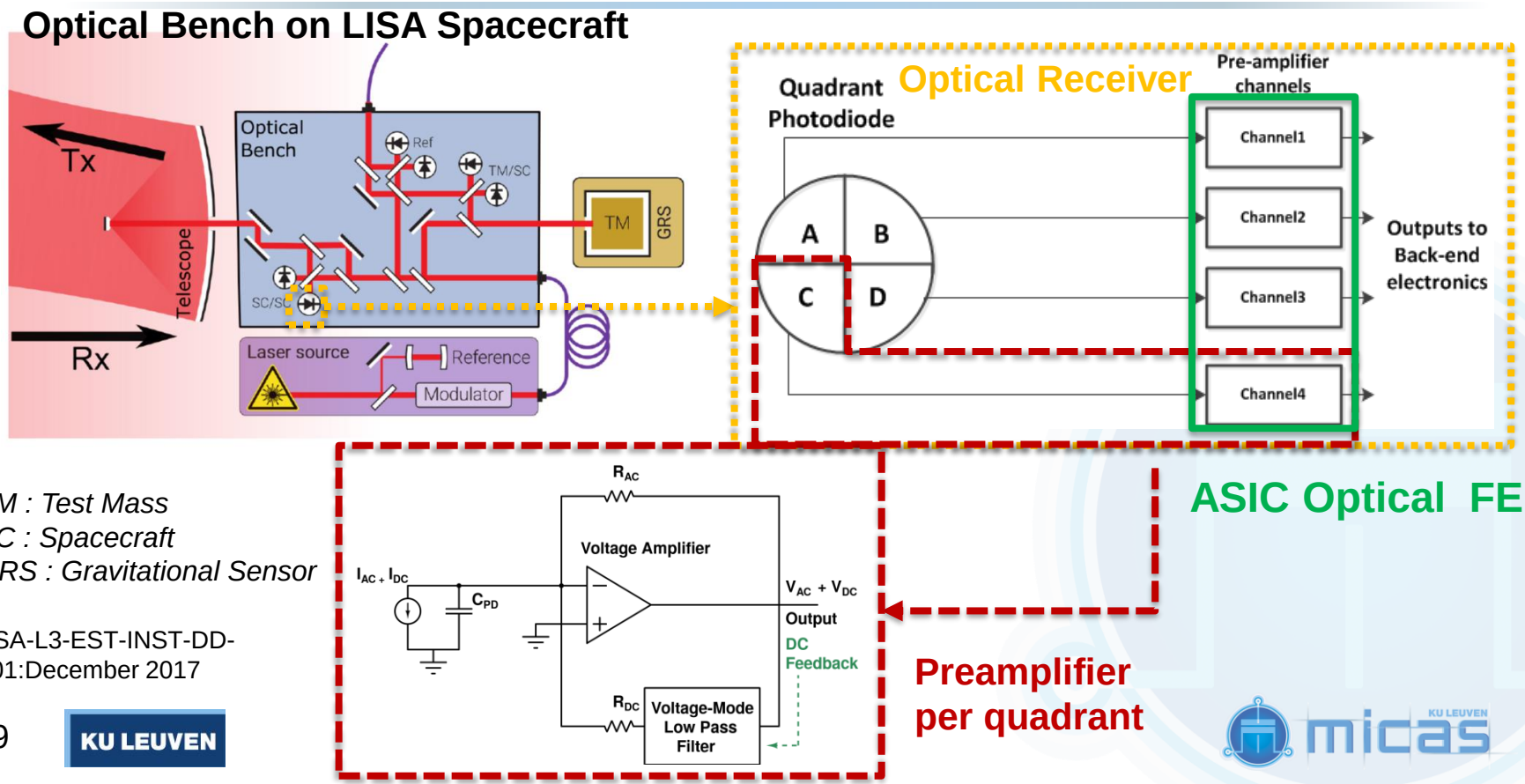
# Optical Front-End Electronics (FEE) for LISA




*TM : Test Mass*
*SC : Spacecraft*
*GRS : Gravitational Sensor*

ESA-L3-EST-INST-DD-001:December 2017



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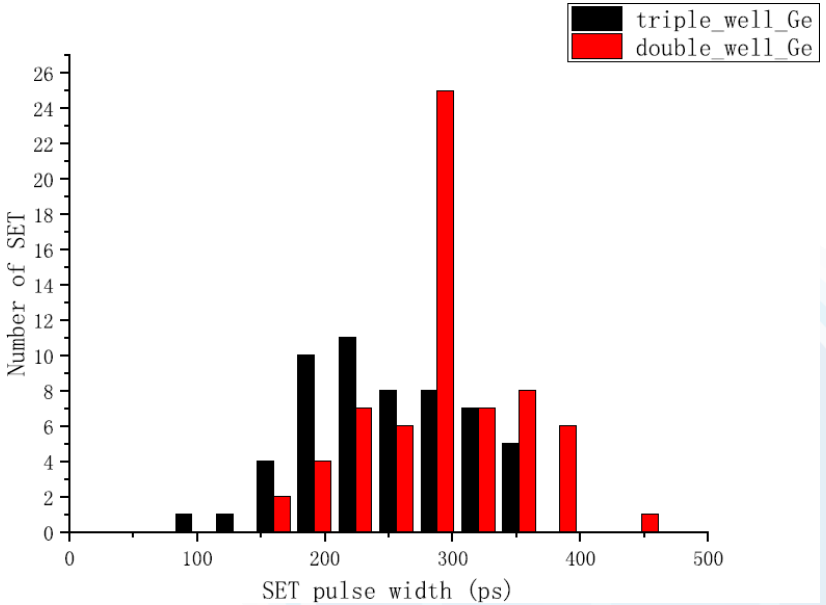
# Radiation induced development challenges

- Insufficient modeling
- Absence of parameters needed to understand topology-based SET effects
- Radiation  models for very high TID levels available which cause overdesign if used




[J.Zhang et al., IEEE Access, Vol.7,  2019]



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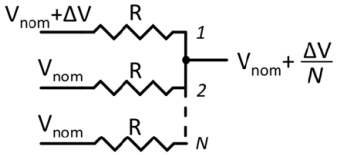
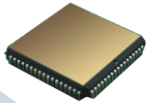
# Radiation-hardened CMOS Design Cycle

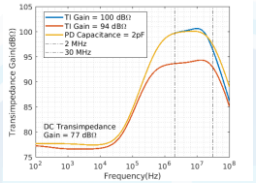



RHBD : Radiation Hardening by Design

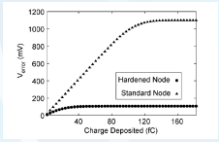
ASIC Design



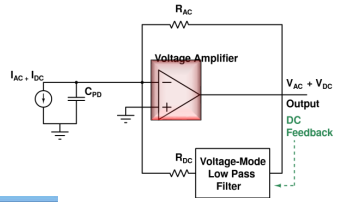
Performance Measurements without radiation




Performance Measurements with radiation




Identifying circuit blocks affected by radiation




Identification of RHBD techniques to be employed



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# Current development focus

- **LISA**:
  - Tackle noise requirement using suitable architectures and radiation effects study
  - Use analysis to implement RHBD techniques to ensure performance reliability
- **ET- LF**:
  - Deep-cryogenic characterization to obtain a working compact model
  - Use the compact model to design a cryo-CMOS MEMS interface
  - In the meantime, design the cryo-MEMS sensor

# Conclusion

- Integrated circuits enable compact and low-power implementations of functional blocks
- Appropriate modeling of environmental factors further assists in performance and reliability
- Overall, a customized solution **tailored on the application** that is able to exceed desired performance
- Research in IC domain is typically 15 years ahead of industrial products!

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# Supplementary slides

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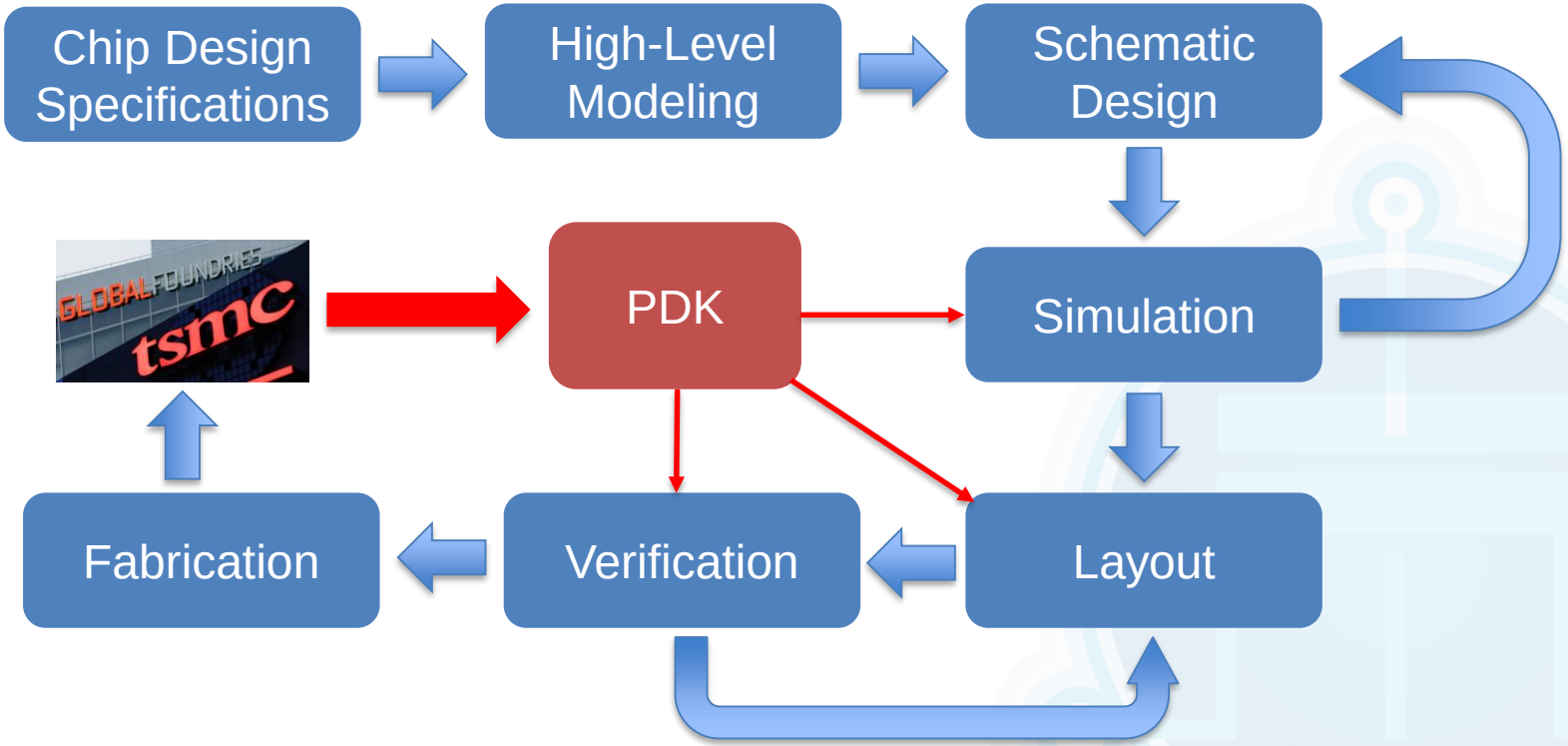
# Chip Design Workflow



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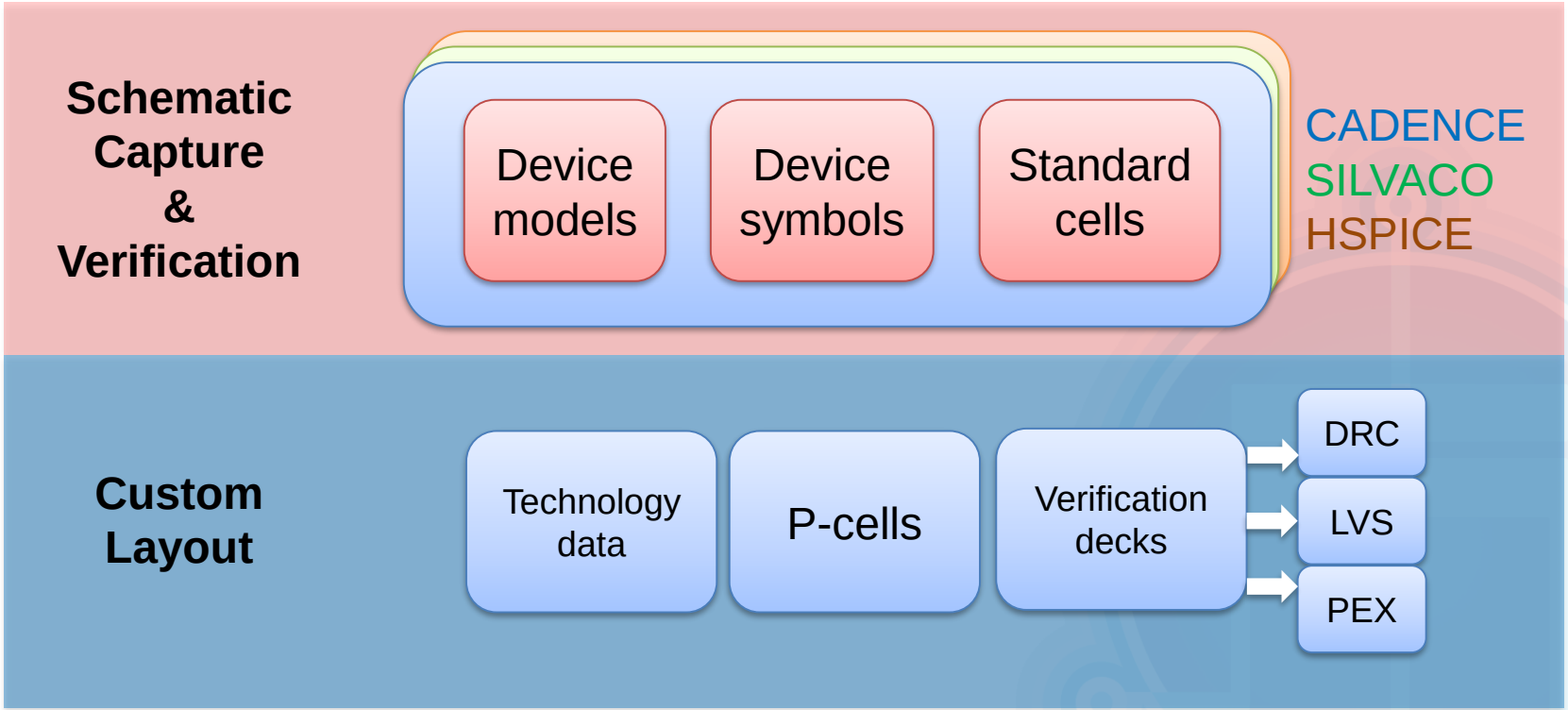
# Process Design Kits (PDKs)



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