DUNE @ BNL

Jay Hyun Jo

January 16, 2025

Brookhaven
National Laboratory

DUNE: next-generation long-baseline neutrino experiment

Far Site

- *1300km from the proton source*
- *very large LAr TPCs (each 17 ktons)*
- *underground in South Dakota*

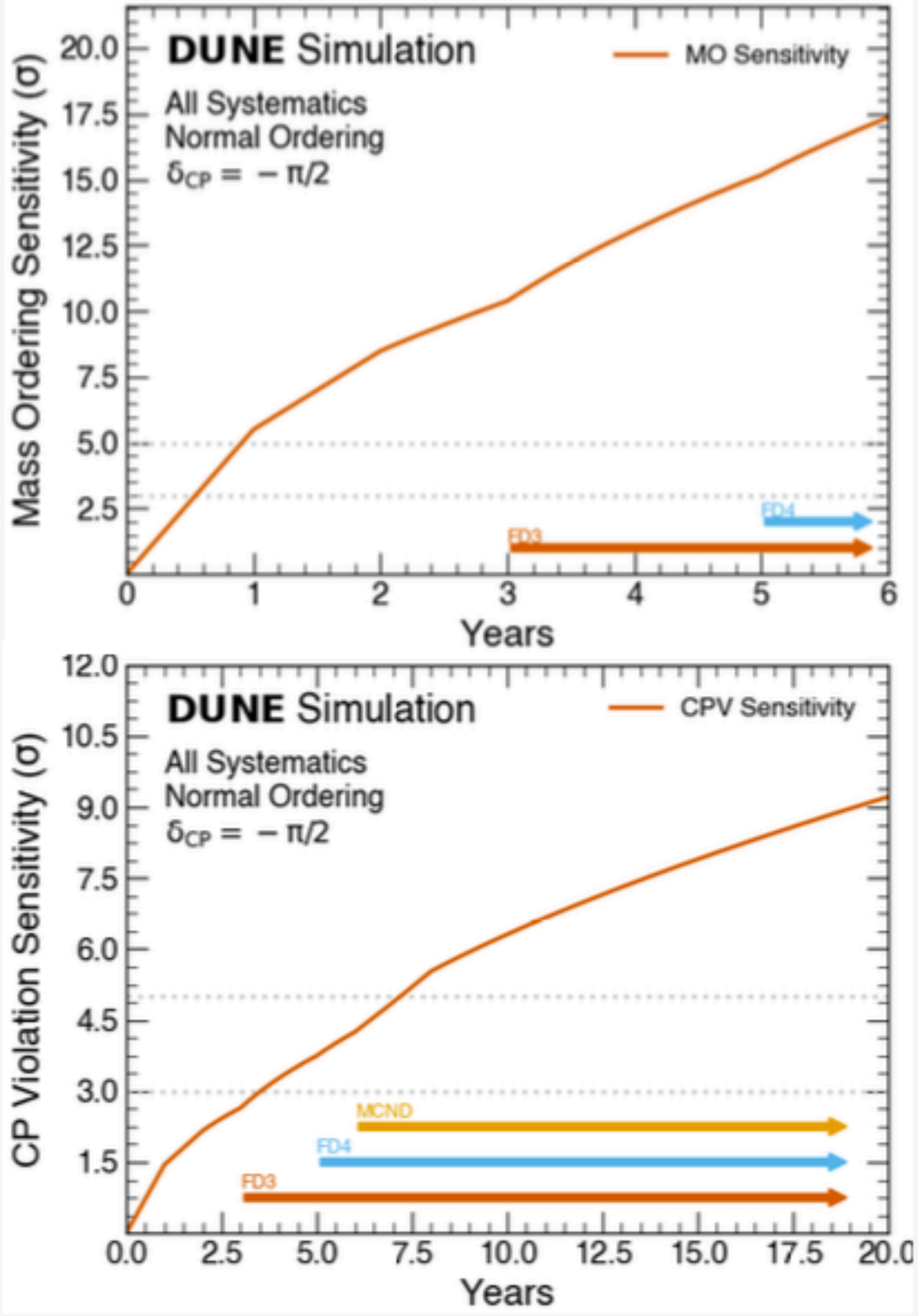
Near Site

- *550m from proton source*
- *on-site at Fermilab*
- *both stationary & moveable detectors*

DUNE: sensitivity & construction schedule

C. Marshall

Eur. Phys. J. C 80, 978 (2020)

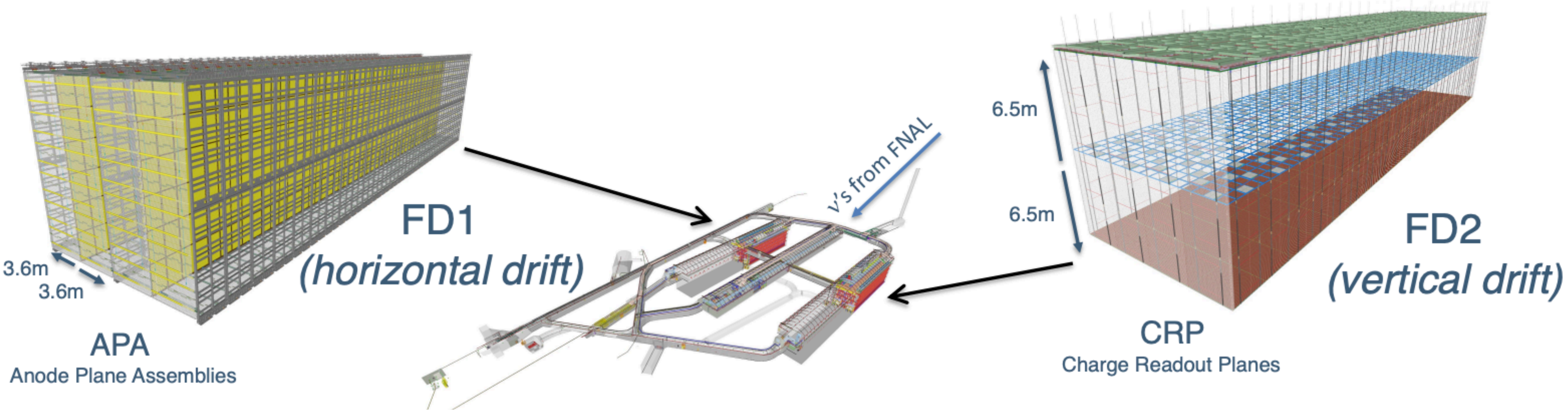


- For best-case oscillation scenarios, DUNE has
  - >5σ mass ordering sensitivity in 1 year
  - >3σ CPV sensitivity in 3.5 years

- Far site excavation is complete
- Next: Building & Site Infrastructure work until mid-2025
- Cryostat warm structure is on its way to US from CERN to be installed in 2025-26
- Far Detector installation in 2026-27
- Purge and fill with argon in 2028
- Physics in 2028 or early 2029
- Beam physics with Near Detector 2031

DUNE Phase I Far Detector

- Phase 1 will include caverns for 4 detector modules in South Dakota and 2 far detector modules, each 17 kton of LAr, the largest LAr TPCs ever constructed.
  - *FD1: horizontal drift*
  - *FD2: vertical drift*



wire readout

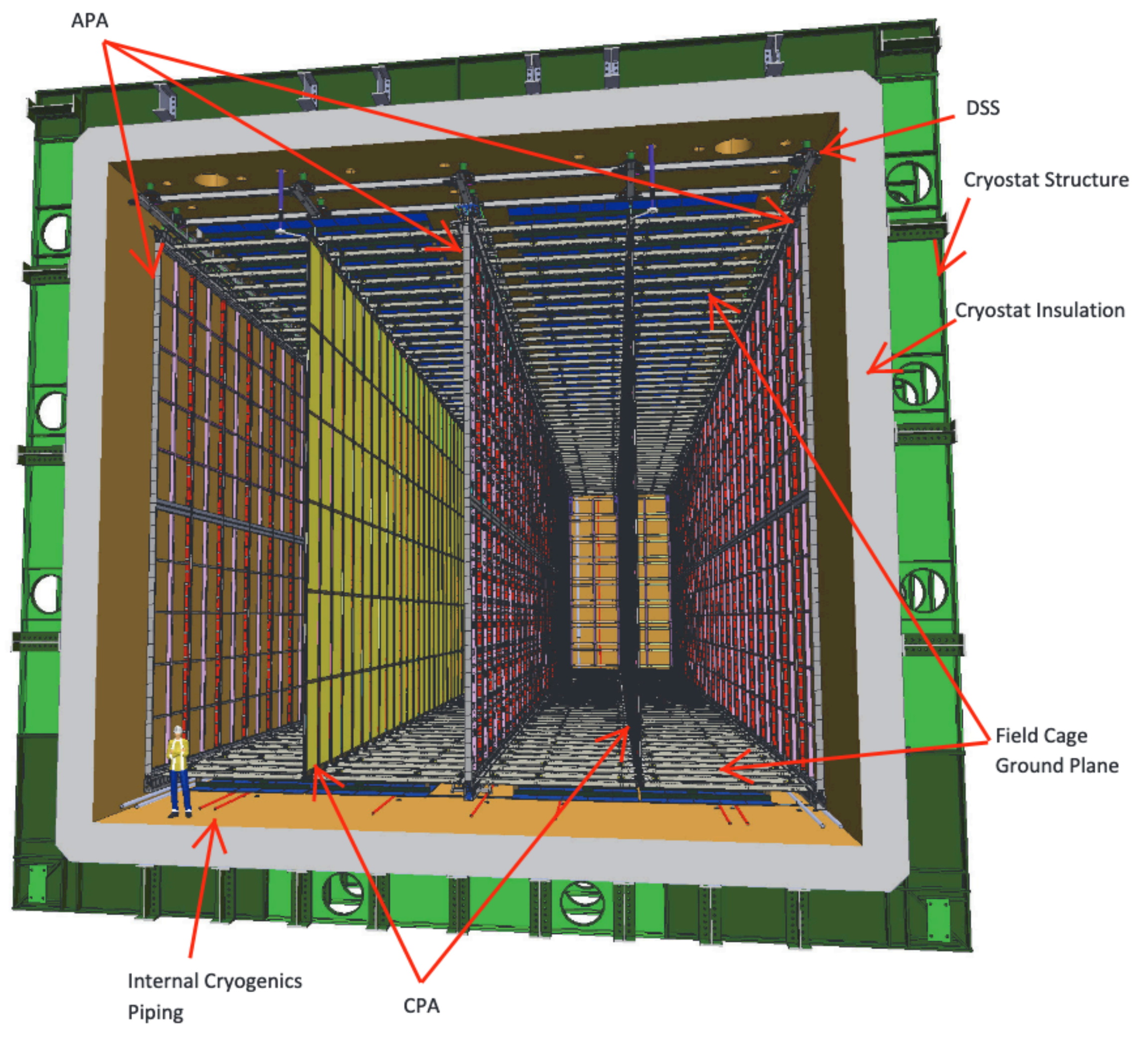
PCB readout

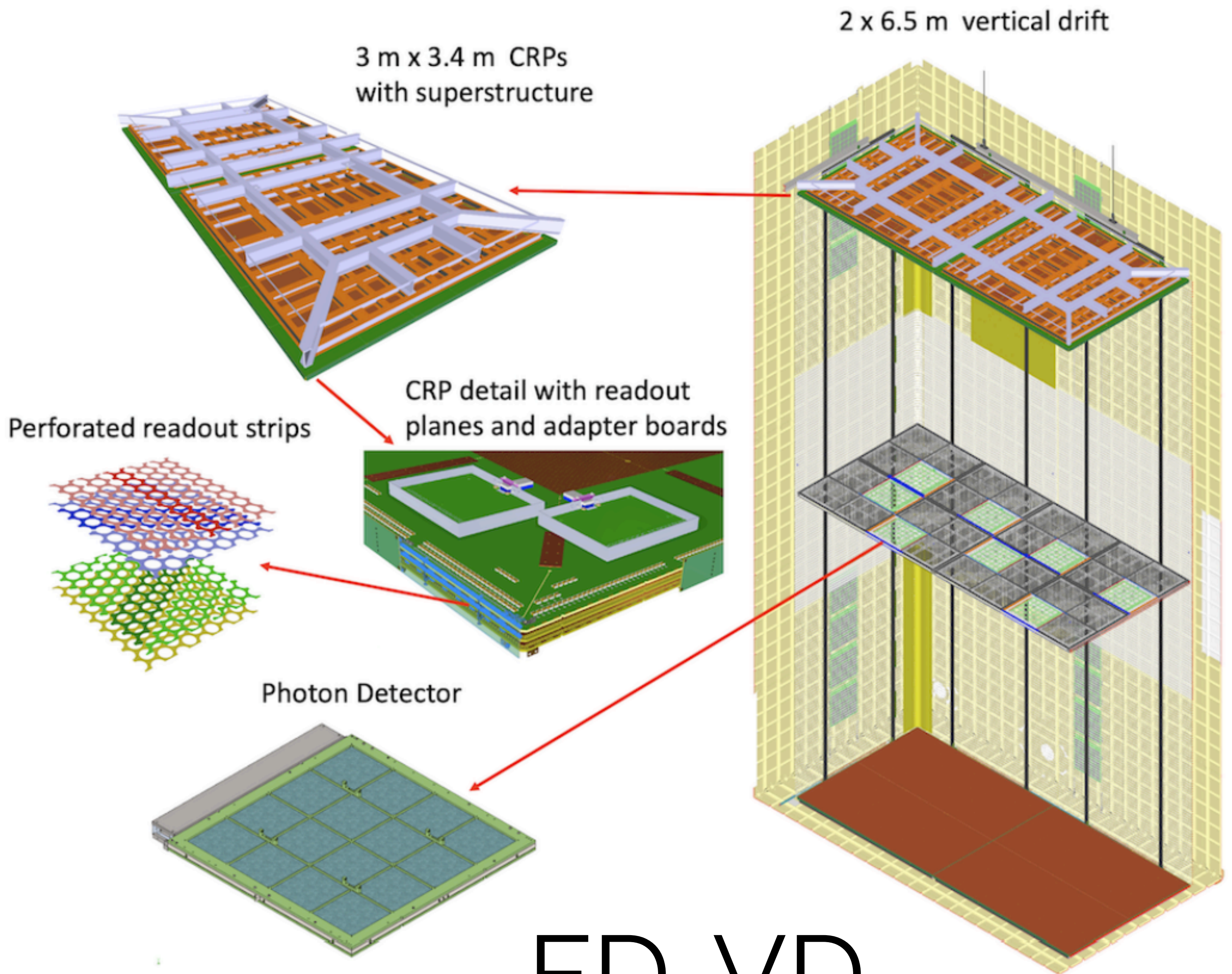
Critical Steps @ BNL

Steve Kettell

- validate technology and analysis to secure DUNE FD-VD and FD-HD
  - **cold electronics (CE)**
    - validate with MicroBooNE, SBND, ProtoDUNE
  - **low noise system design**
    - validate with MicroBooNE, ProtoDUNE
  - **effective 3D reconstruction with Wire-Cell**
    - validate with MicroBooNE, with further improvements for DUNE
  - **demonstrate oscillation analysis**
    - validate with MicroBooNE, with improvements in SBN for DUNE

FD-HD





FD-VD

Hardware

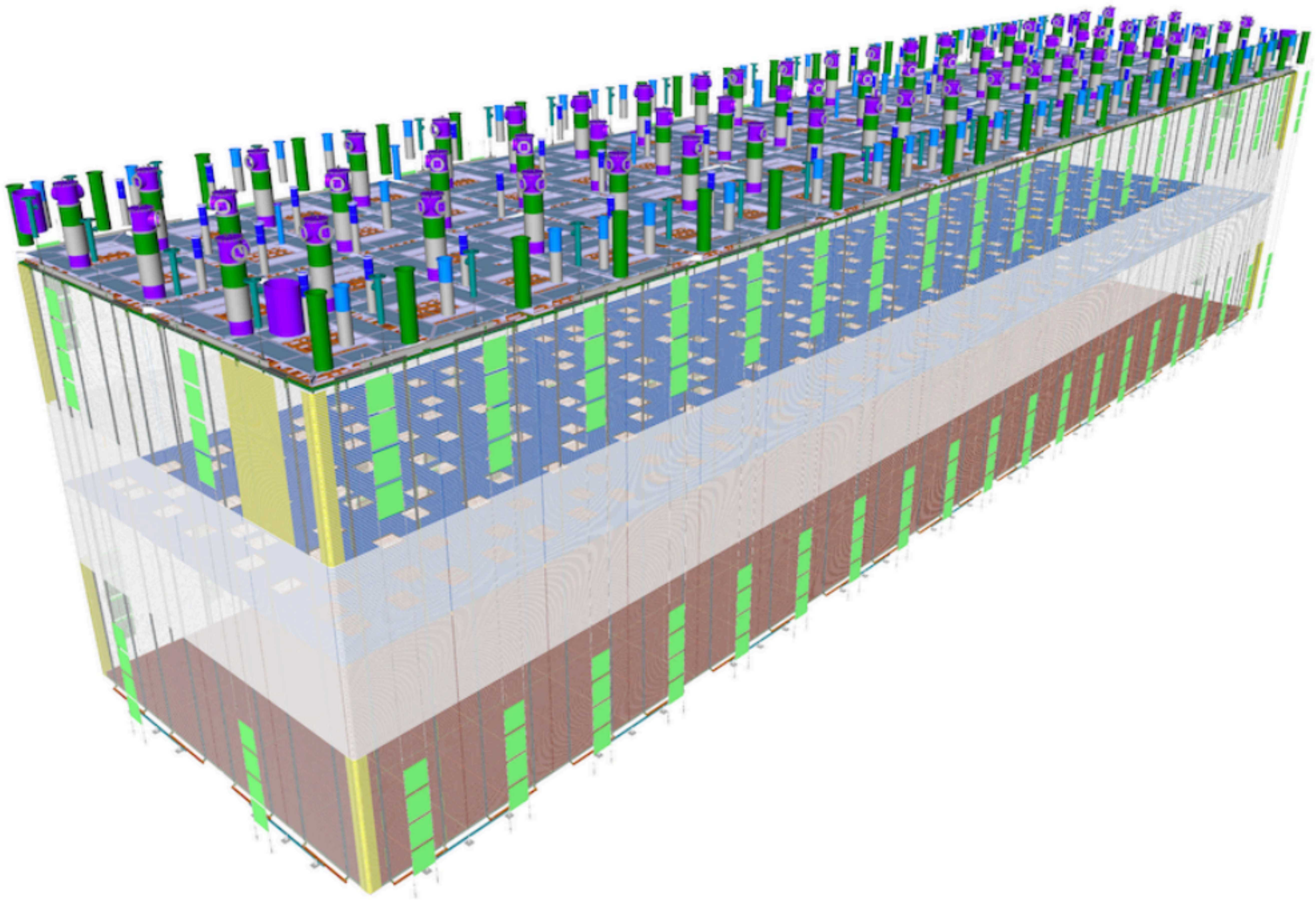
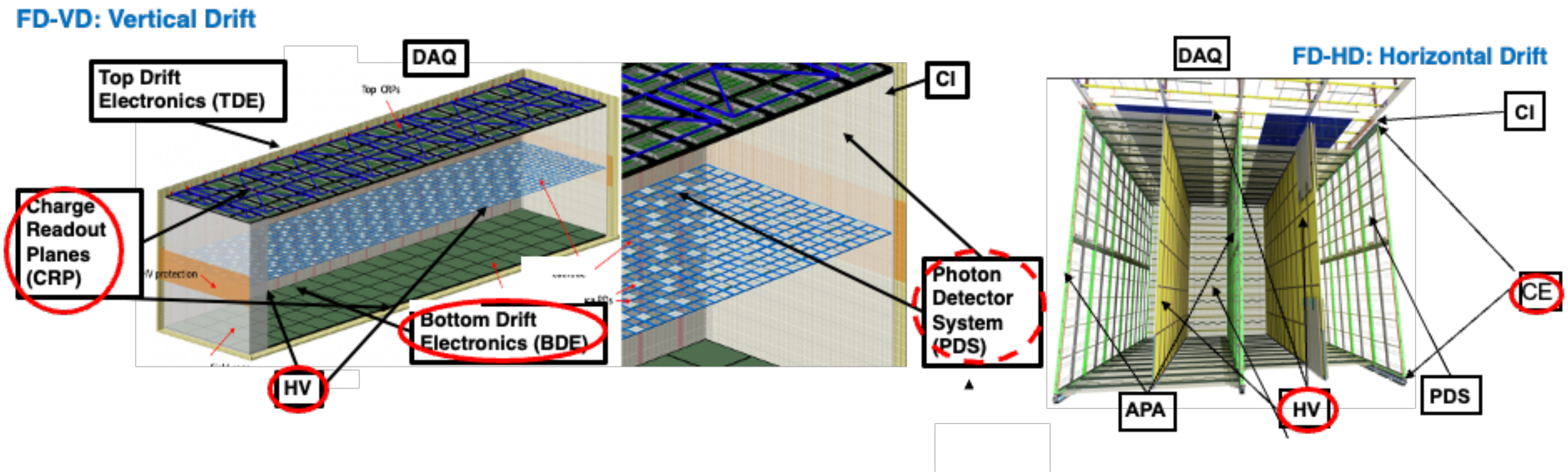


Figure 1.3: Perspective view of the FD2-VD detector.

BNL deliverables

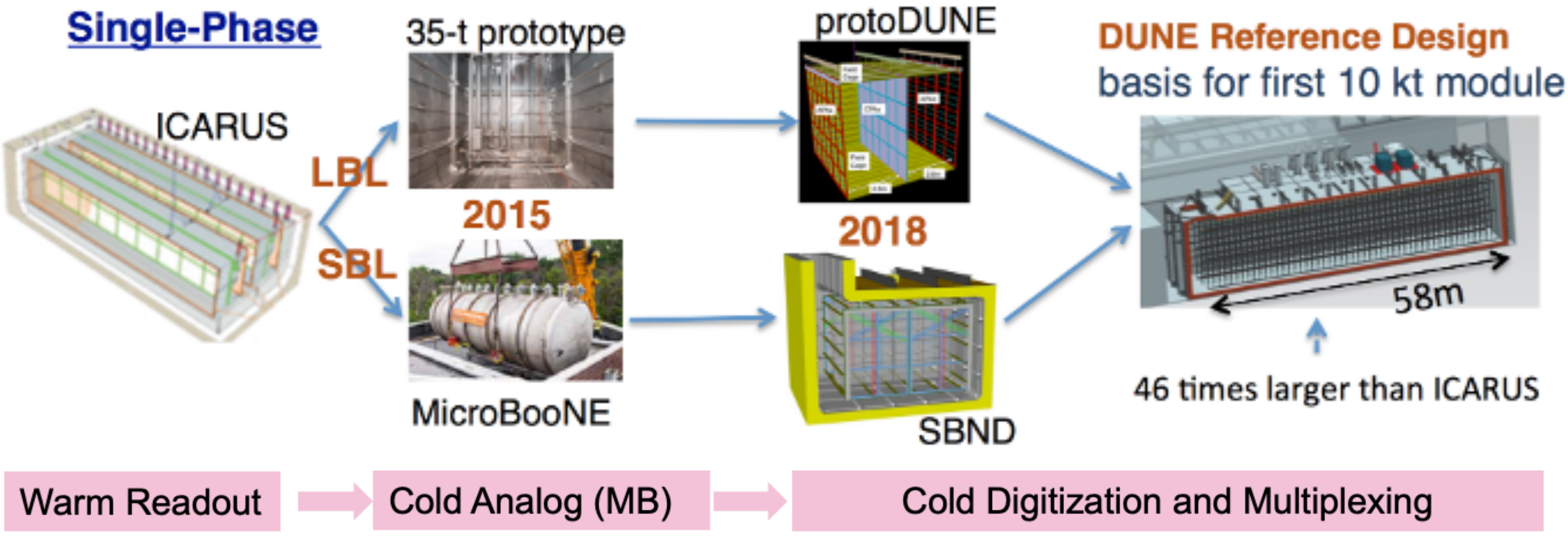
Steve Kettell



- Major BNL deliverables
  - FD-VD: bottom charge readout plane, bottom drift electronics, high voltage
  - FD-HD: cold electronics, high voltage

Cold Electronics

Shanshan Gao

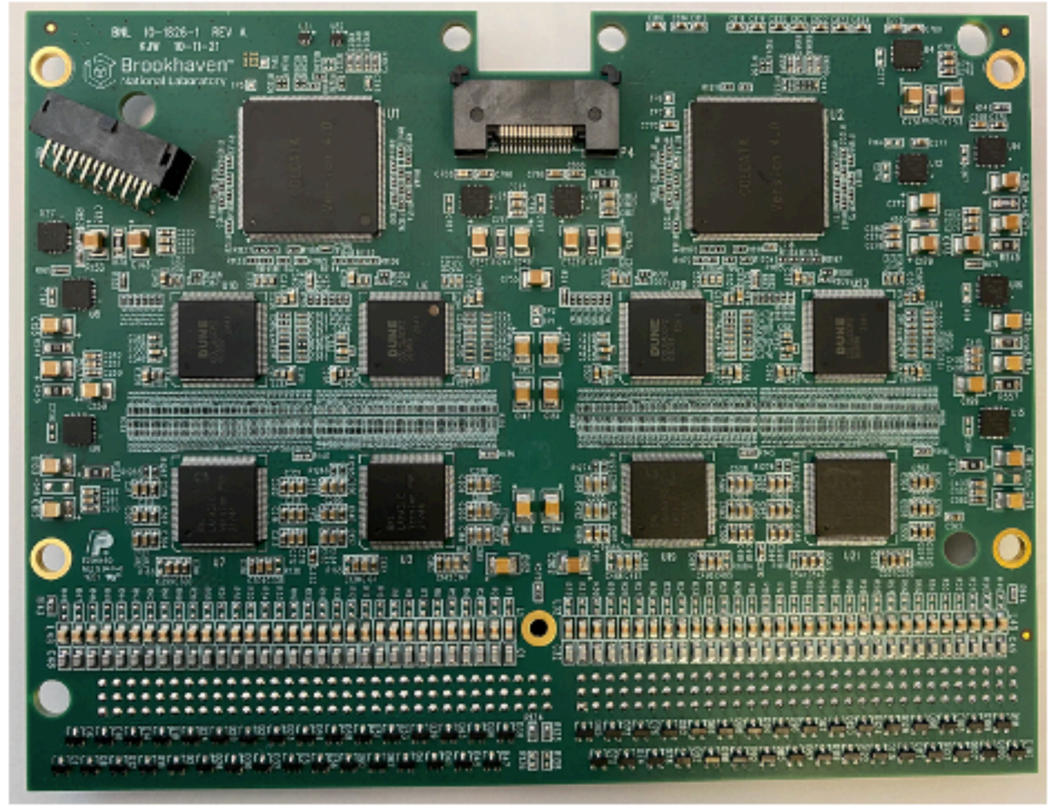


- CE is a key technology for large LArTPCs, with its very low noise and minimal cryostat penetration
  - "The cold electronics that it remains an optimal solution for very large TPC": Velkjo Radeka et al.
  - BNL is leading TPC readout electronics/system desing

CE testing @ BNL

Shanshan Gao

- FD1: 150 APAs, 384,000 channels
- FD2: 80 bottom drift CRPs, 245,760 channels
- testing ASIC chips & FEMB in systematic, rigorous, and precise way is important



FEMB with **three** cryogenic-qualified ASICs (LArASIC, ColdADC, COLDATA) well addresses the long lifetime (30 years) and reliability requirements of DUNE far detector.

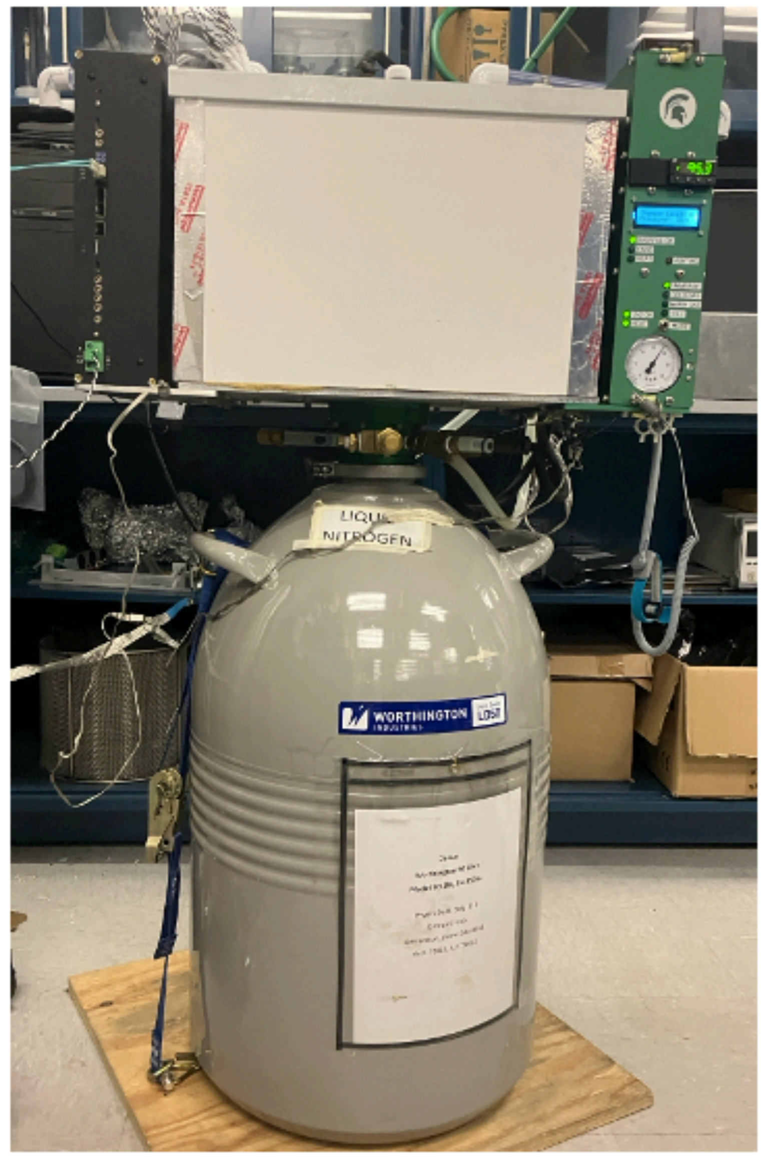
	FD1	FD2
anode unit	150 APA	80 CRP
Electrodes (charge readout)	384,000	245,760
LArASIC	24,000	15,360
ColdADC	24,000	15,360
COLDATA	6,000	3,840
FEMB Assembly *	3,000	1,920
Cold cable bundles	150	80
Feed-through	75	40
CE flanges	150	80
WIEC crate	150	80
WIB	750	480
PTC	150	80
PTB	150	80

*: require at least 10% spares

Shanshan Gao

DUNE CE FEMB QC

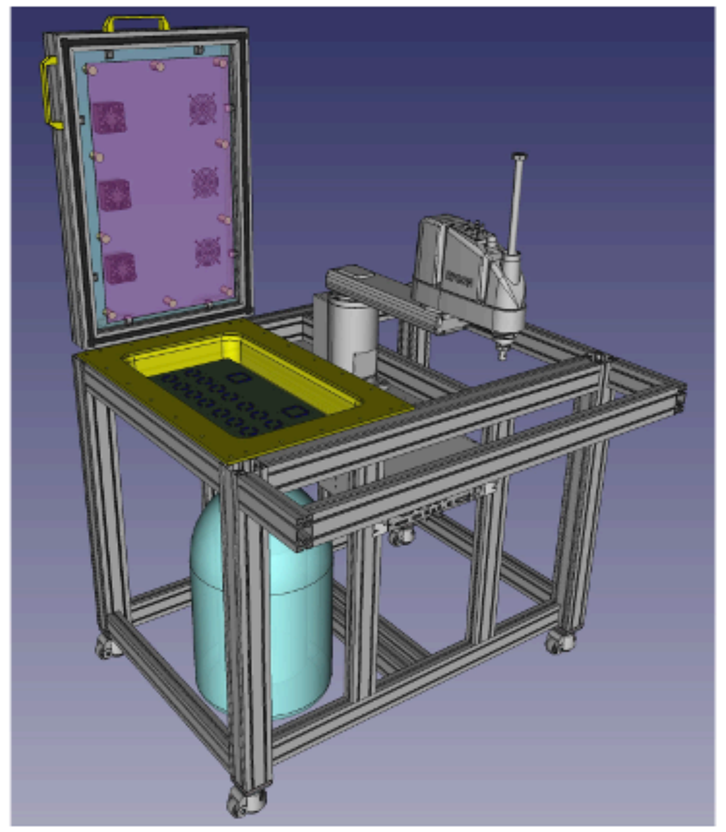
- QC activities will be monitored and led by the **TPC electronics consortium**
  - The **same hardware setup** CTS and the same QC procedure will be distributed to all test sites.
  - FEMB QC based on CTS can perform thermal cycle testing (room temperature to liquid nitrogen) for up to 4 FEMBs simultaneously



QC Test Setup Hardware

DUNE CE ASIC QC

An automatic ASIC cryogenic test stand is being developed to test over 100k chips for DUNE FD1 and FD2-BDE



The RTS comprises:

A commercial robot to pick and place the ASICs from trays to test sockets

Test chambers that support the testing hardware.

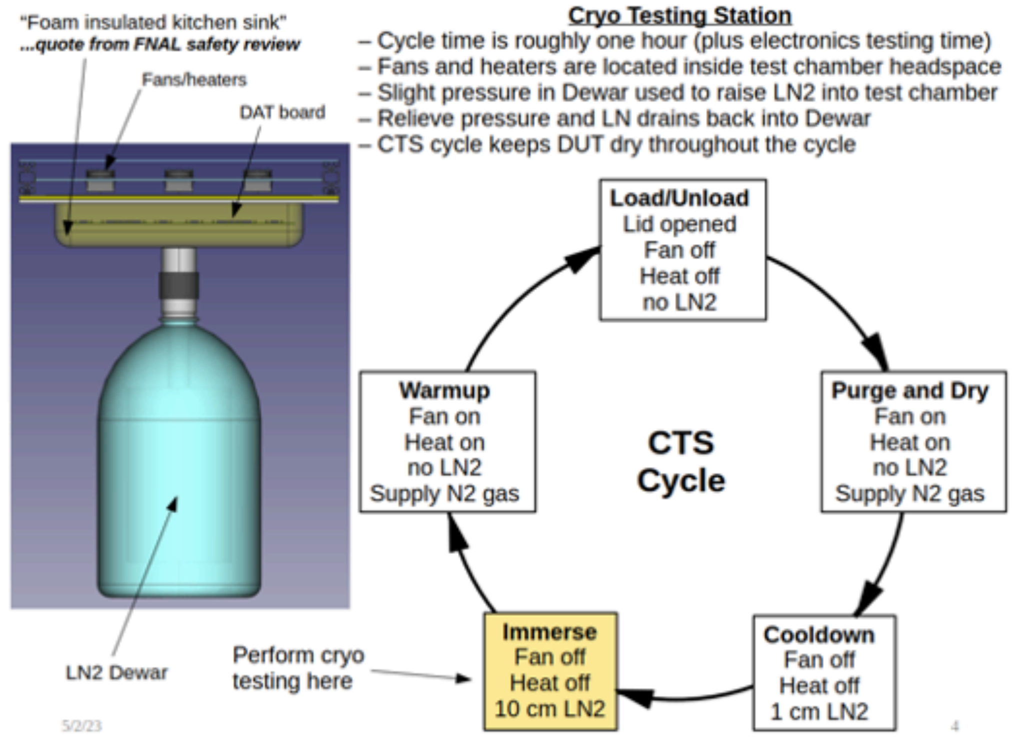
Test chambers are also Faraday enclosures.

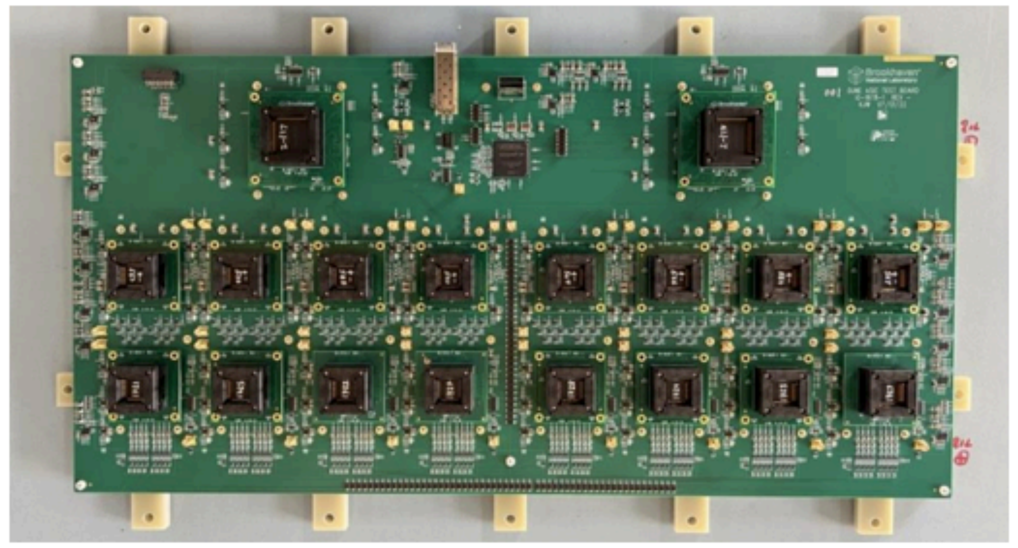
A cryogenics system that can fill and drain the test chambers.

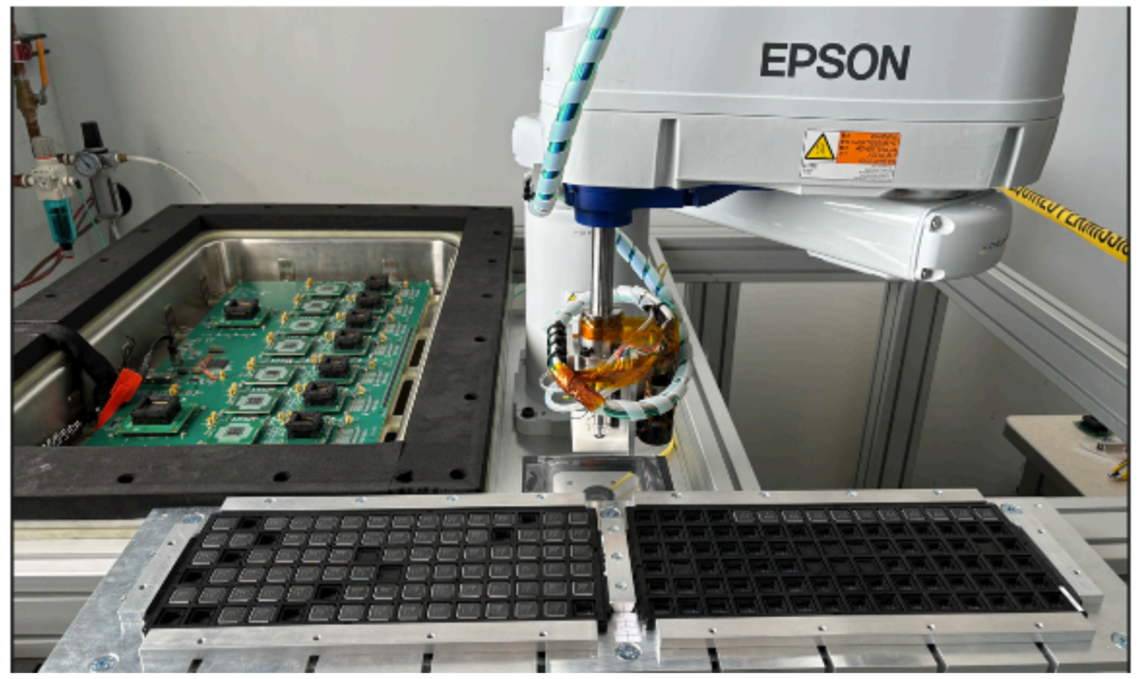
An aluminum strut framework to hold this all together.

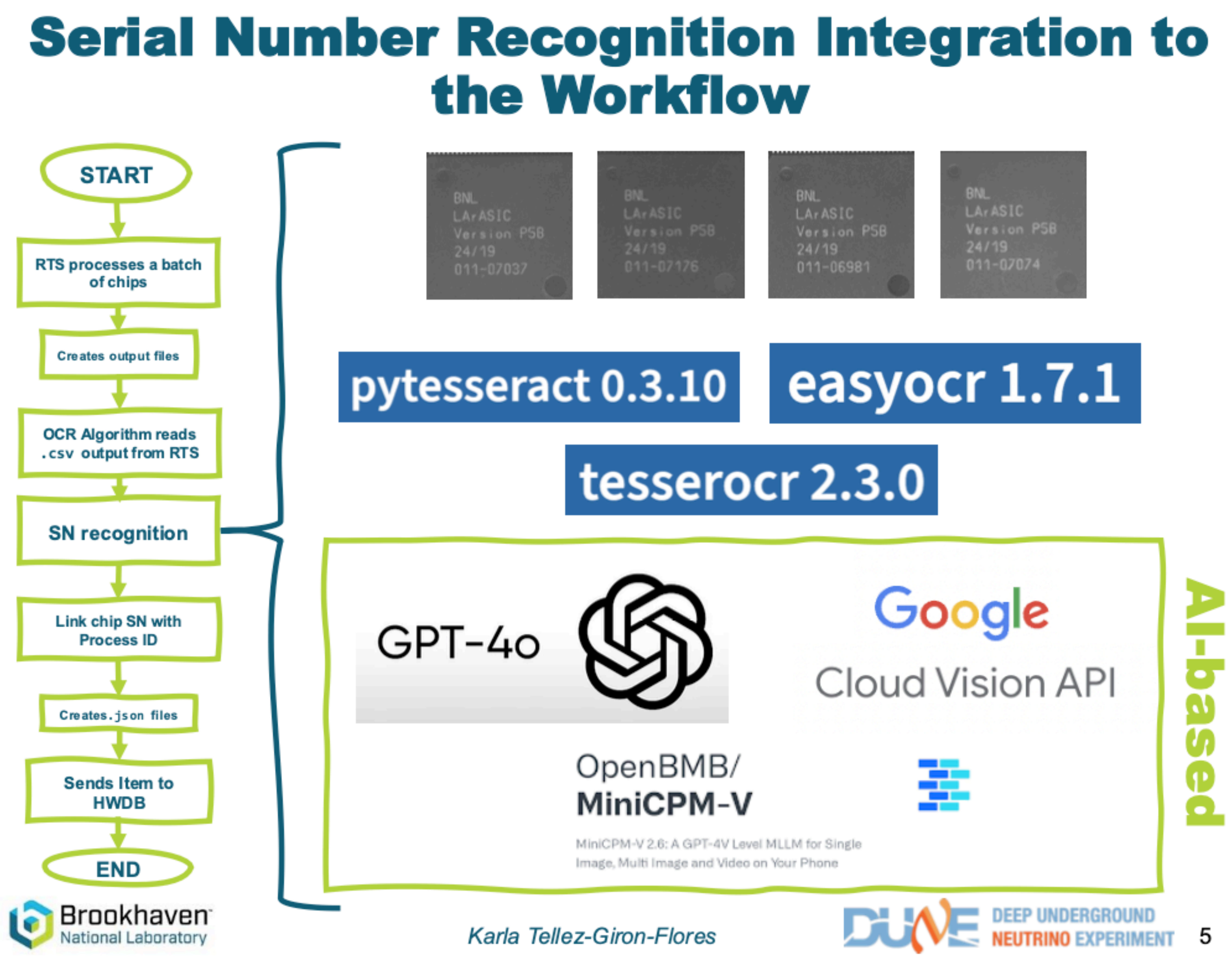
An upper level to the strut framework to provide a safety enclosure with access doors (not shown).

RTS system has two test chambers, only one is shown here.





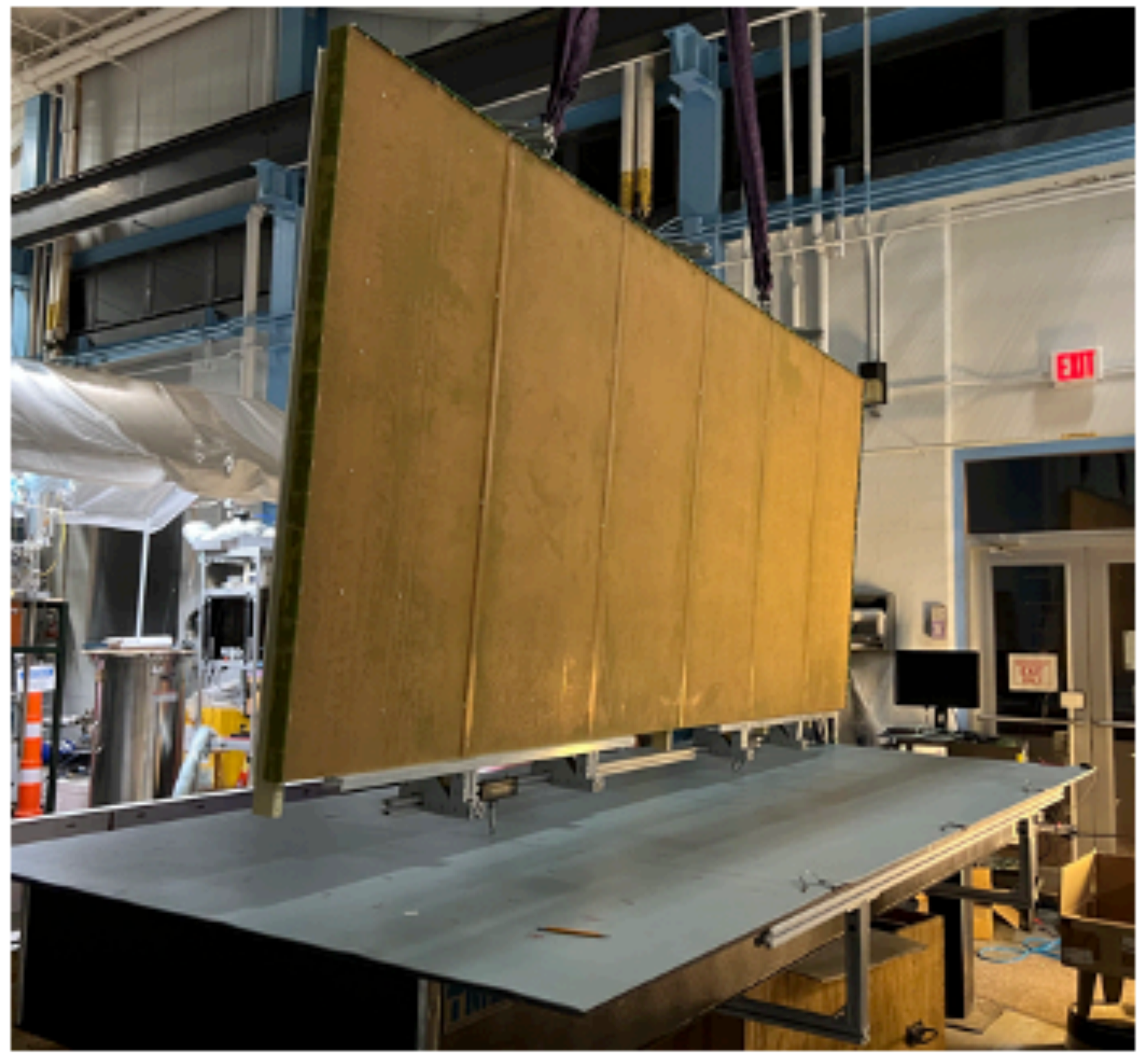


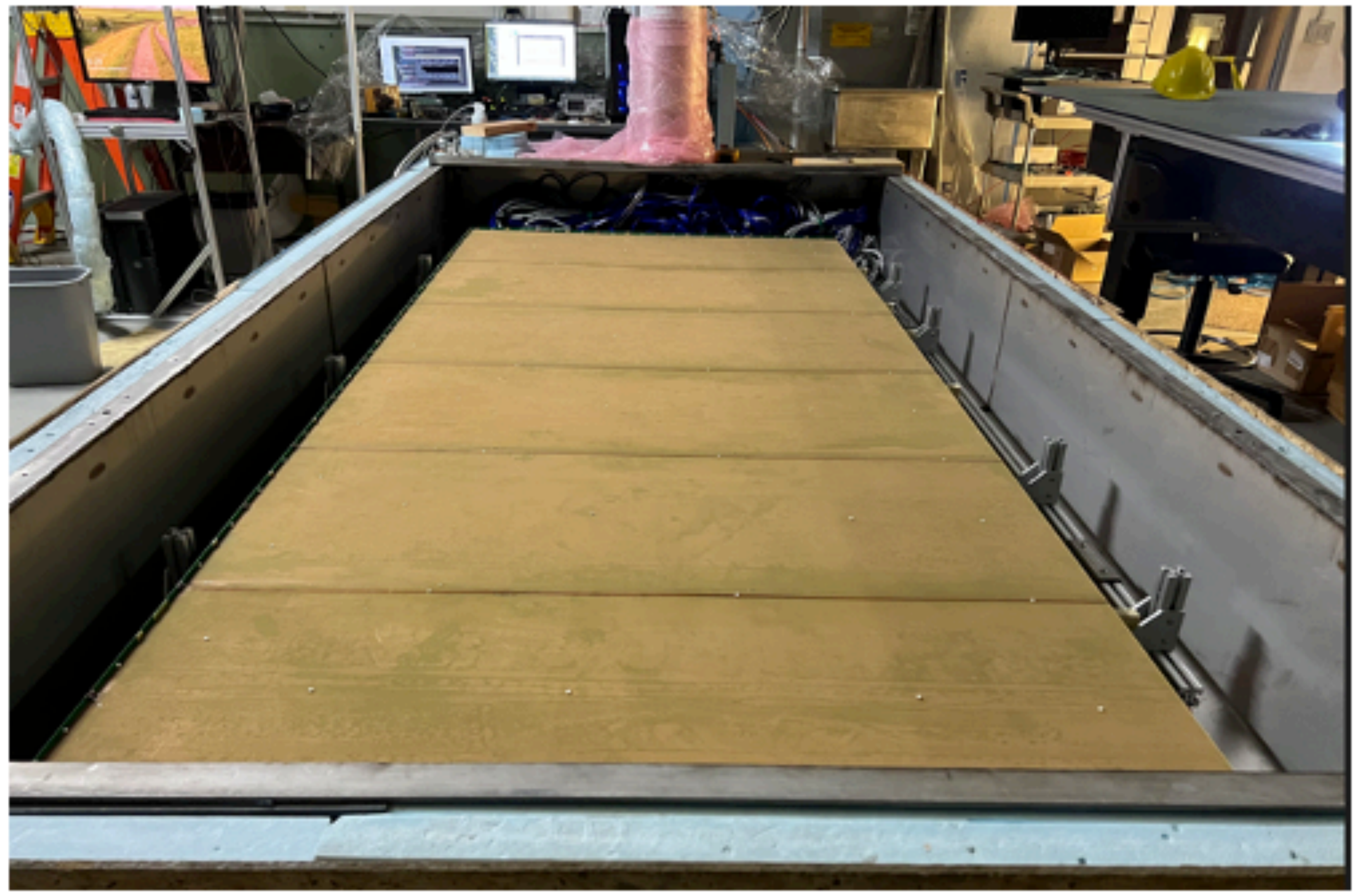

Serial Number Recognition Integration to the Workflow
START
RTS processes a batch of chips
Creates output files
OCR Algorithm reads .csv output from RTS
SN recognition
Link chip SN with Process ID
Creates.json files
Sends Item to HWDB
END
BNL LArASIC Version P5B 24/19 011-07037
BNL LArASIC Version P5B 24/19 011-07176
BNL LArASIC Version P5B 24/19 011-06981
BNL LArASIC Version P5B 24/19 011-07074
pytesseract 0.3.10
easyocr 1.7.1
tesserocr 2.3.0
GPT-4o
Google
Cloud Vision API
OpenBMB/
MiniCPM-V
MiniCPM-V 2.6: A GPT-4V Level MLLM for Single Image, Multi Image and Video on Your Phone
AI-based
Brookhaven National Laboratory
Karla Tellez-Giron-Flores
DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT
5

Integration test @ BNL

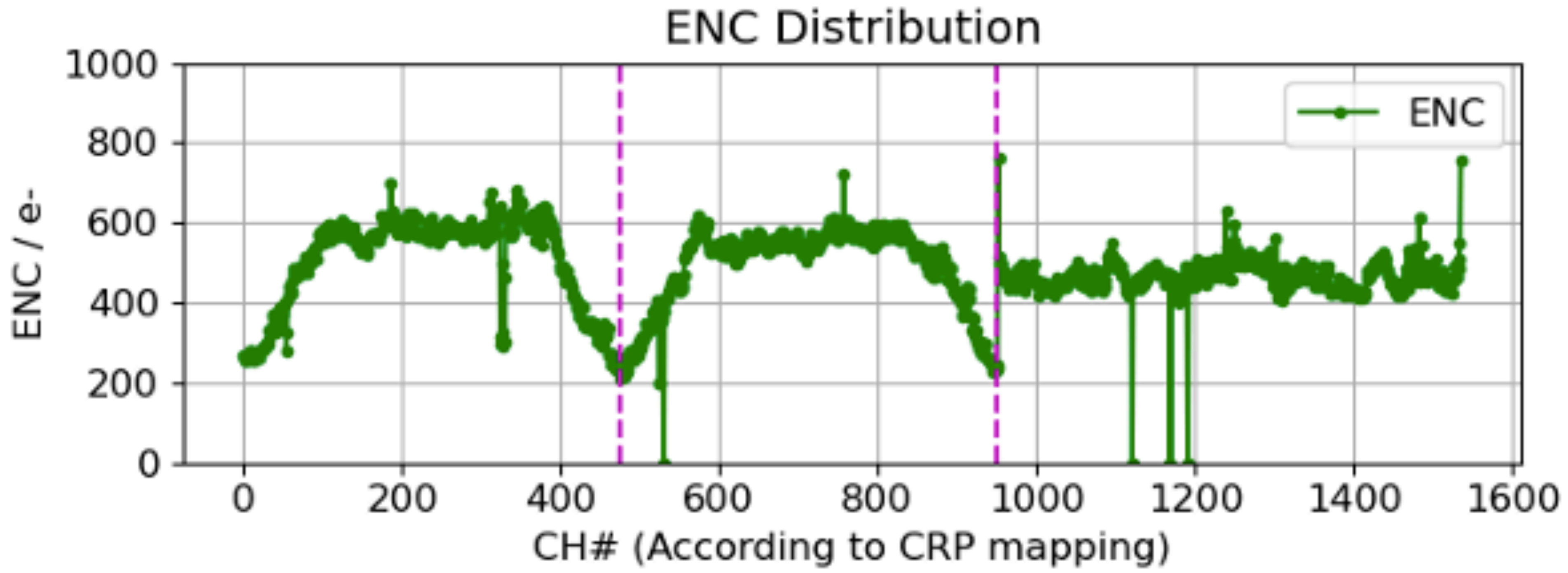
Shanshan Gao

CRP5A: 3.0m x 1.5m, 1536 readout channels (12 FEMBs)





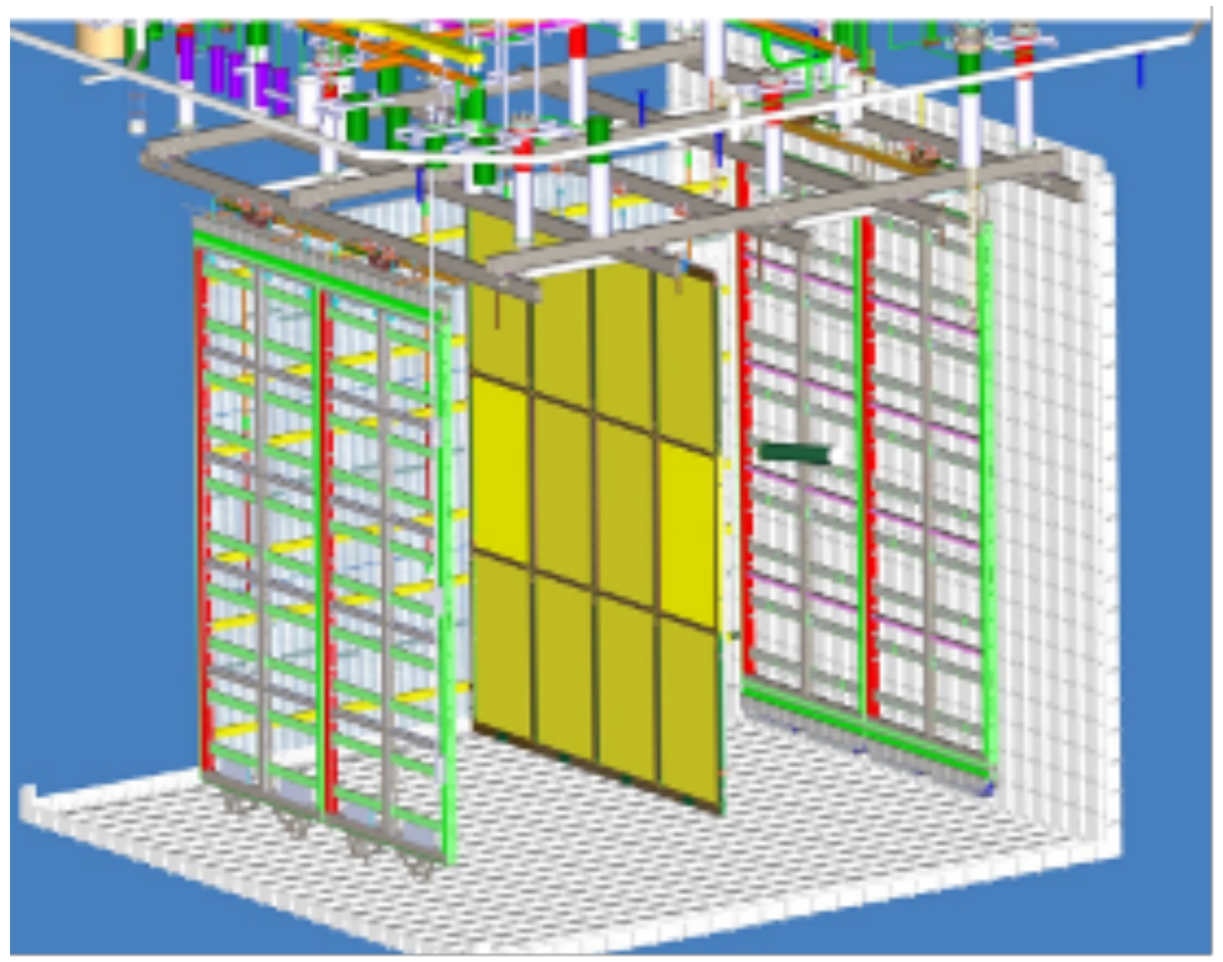
Promising noise performance at LN2



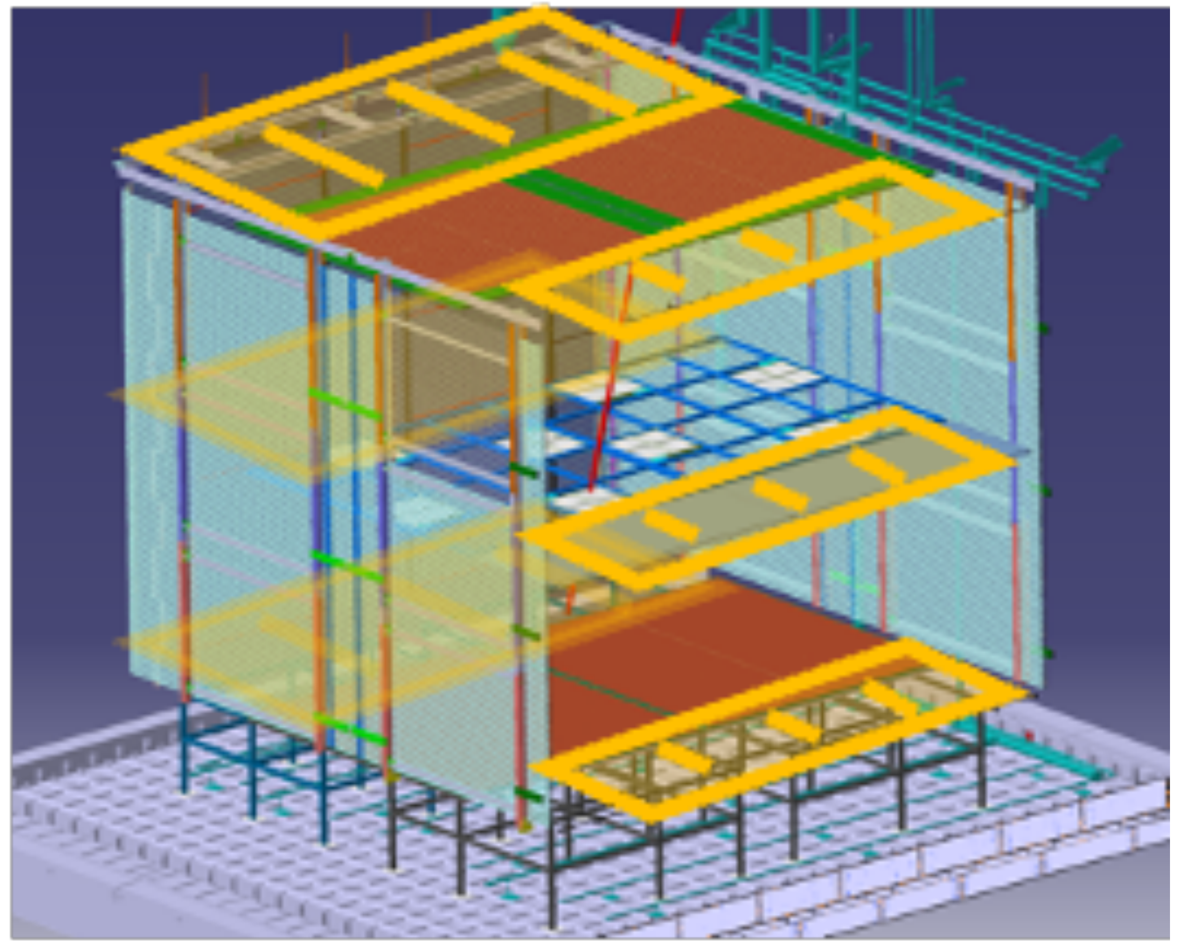
ProtoDUNE-II: HD & VD

Shanshan Gao

- ProtoDUNE Horizontal Design (HD) and Vertical Design (VD)
  - **provide critical validation of technology, detector performance, and long-term stability**
  - PD-HD: 4x APA, 10,240 detector electrodes readout by cold electronics submerged in LAr
  - PD-VD: 2x Bottom CRP, 6,144 detector electrodes readout by cold electronics submerged in LAr
- **BNL focused on Cold Electronics R&D (both electrical and mechanical), production, installation and commissioning**
  - PD-HD: BNL delivered a full set of high-quality cold electronics
  - PD-VD: A CRP2b integration test and CE production at BNL

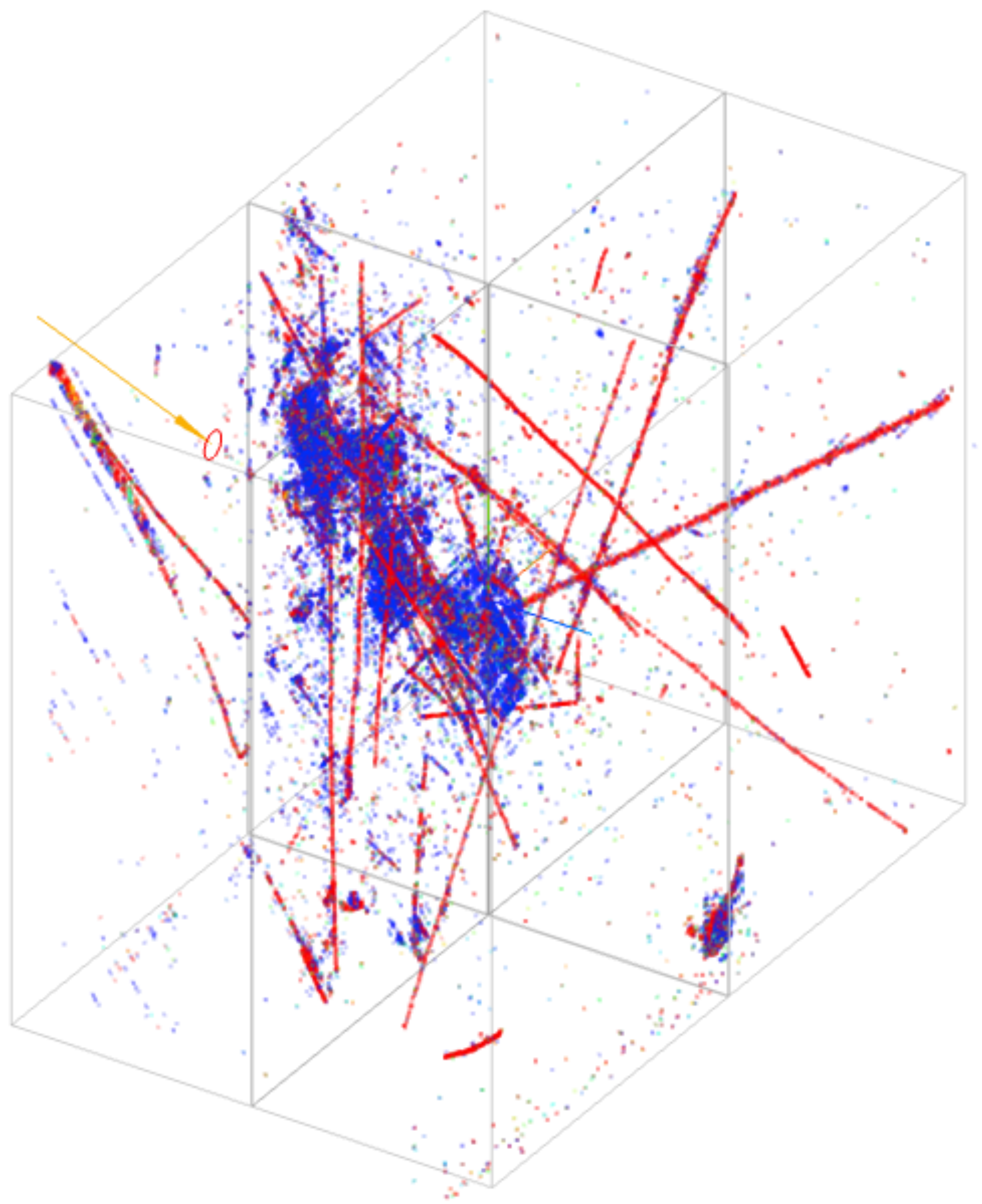


ProtoDUNE HD



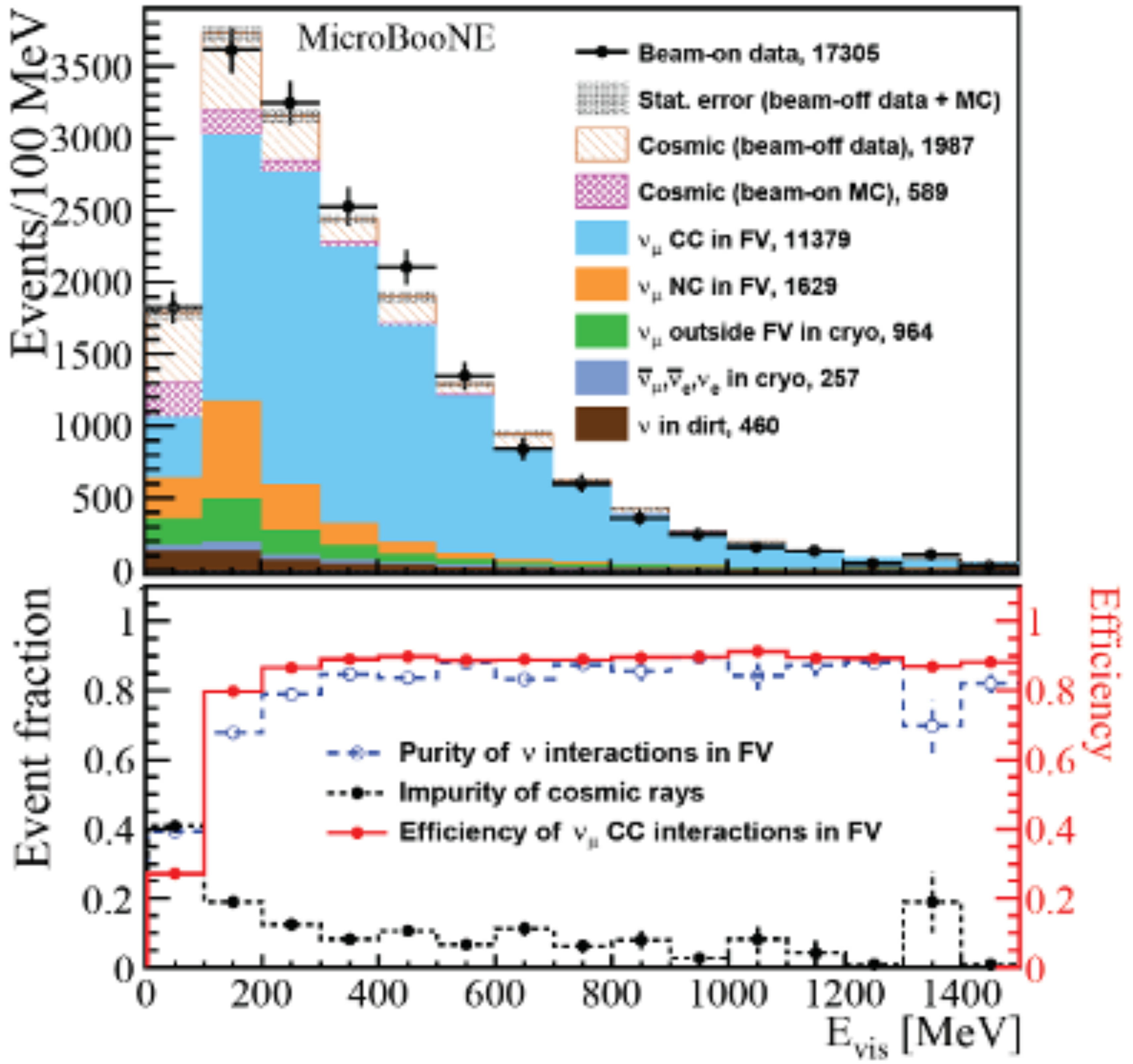
ProtoDUNE VD

Software & Analysis



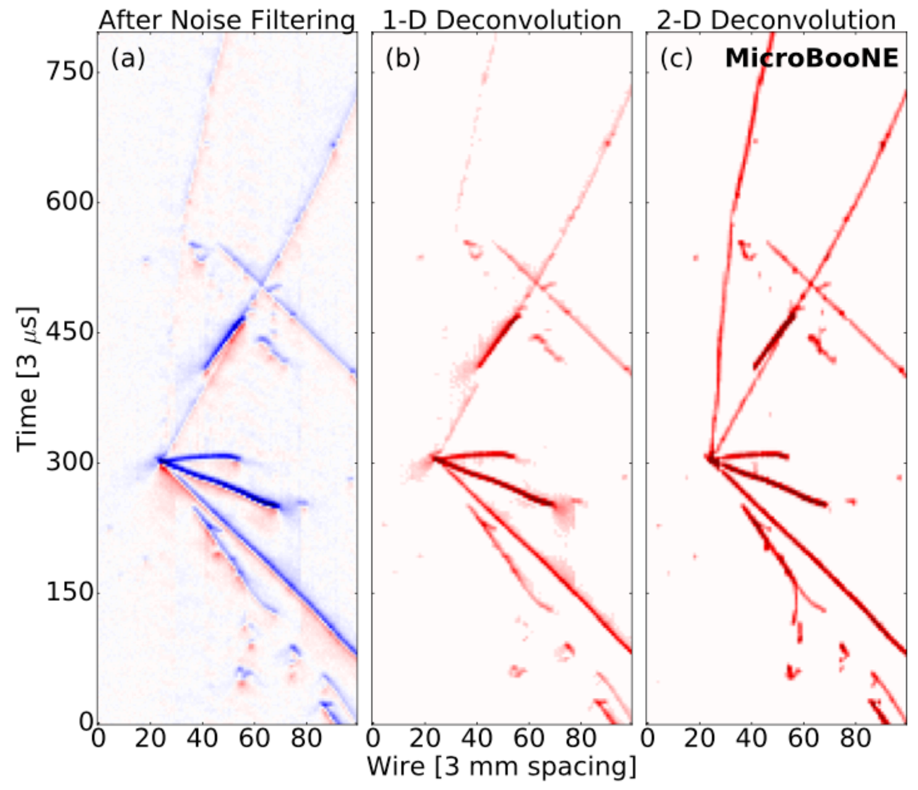
- **Wire-Cell is a collection of software tools for LArTPC that processes from signal processing to event reconstruction and physics analysis**
- WC is the currently the highest performing in terms of neutrino selection efficiency/purity which are fully validated on data with an end-to-end published oscillation and multiple cross section analysis
- *"prototype"* was developed on MicroBooNE, and generalized *"toolkit"* is in the development for DUNE
- BNL is leveraging advanced software/ computational/analysis expertise, developing full reconstruction tool for physics analysis

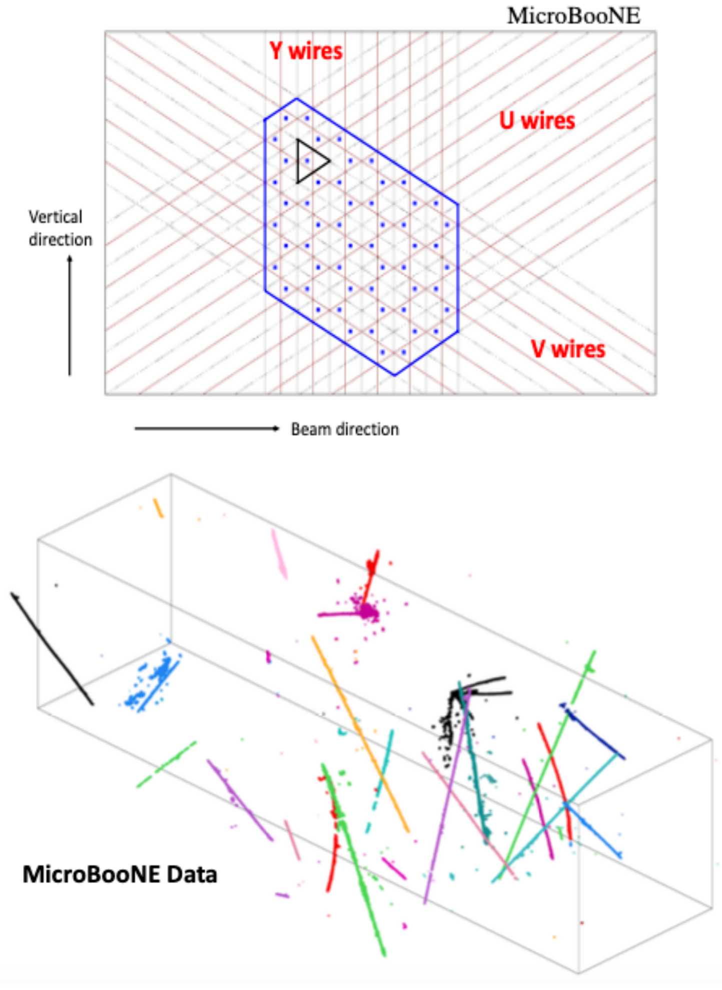
Channels	Reconstruction	Purity	Efficiency	Selected Events	References
CCQE 1e1p	Deep Learning	75%	6.6%	25	PRD 105 112003
1e0p0π	Pandora	43%	9%	34	PRD 105 112004
1eNp0π	Pandora	80%	15%	64	PRD 105 112004
Inclusive 1eX	Wire-Cell	82%	46%	606	PRD 105 112005

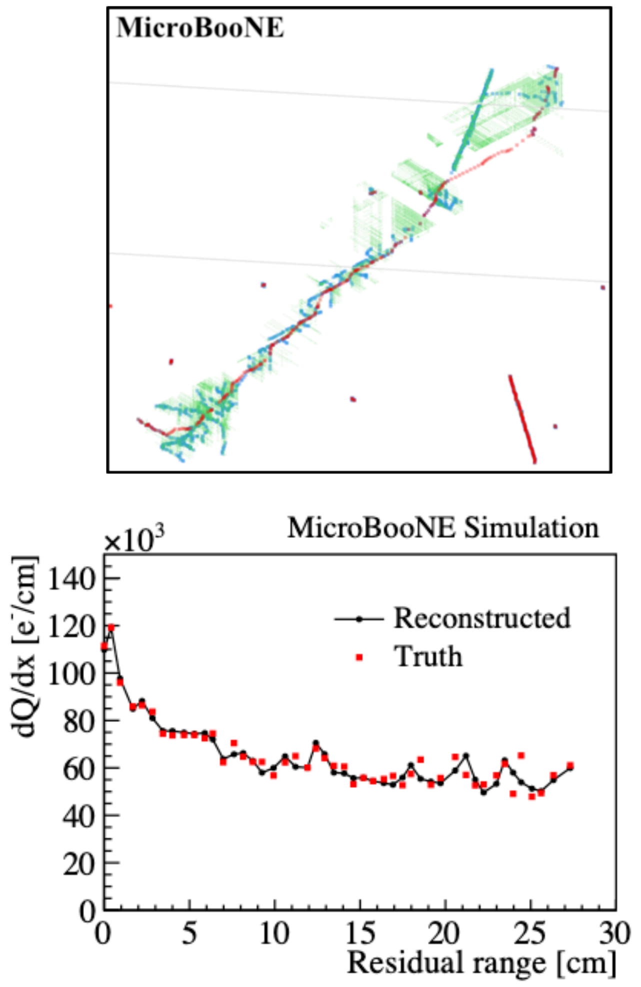


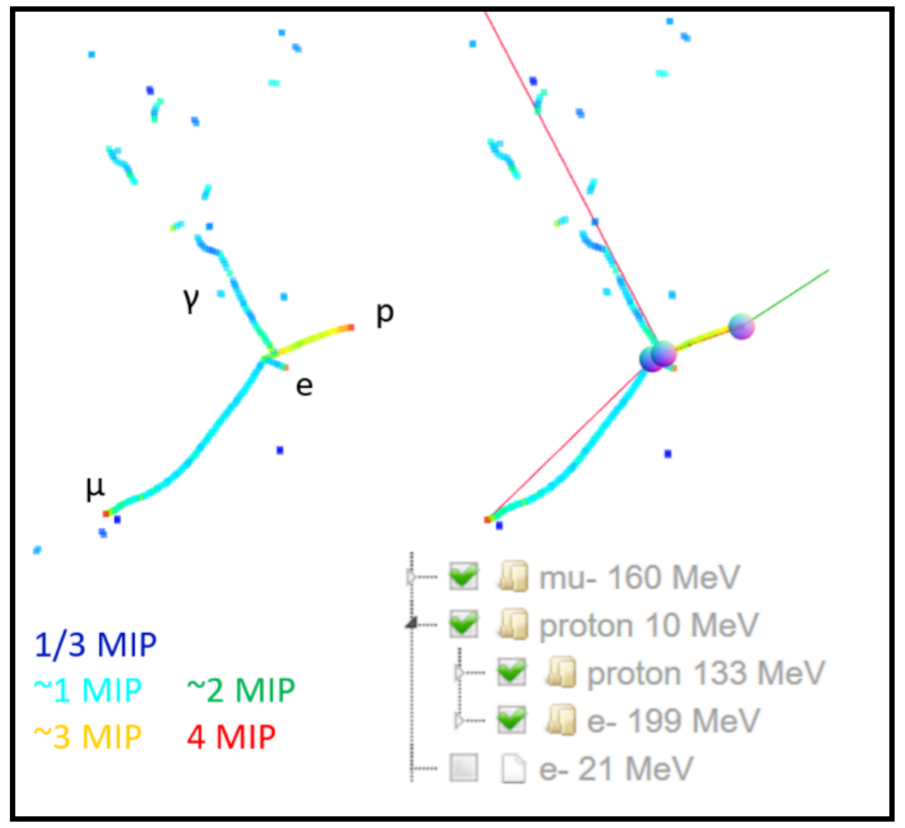
Wire-Cell-Prototype (WCP)

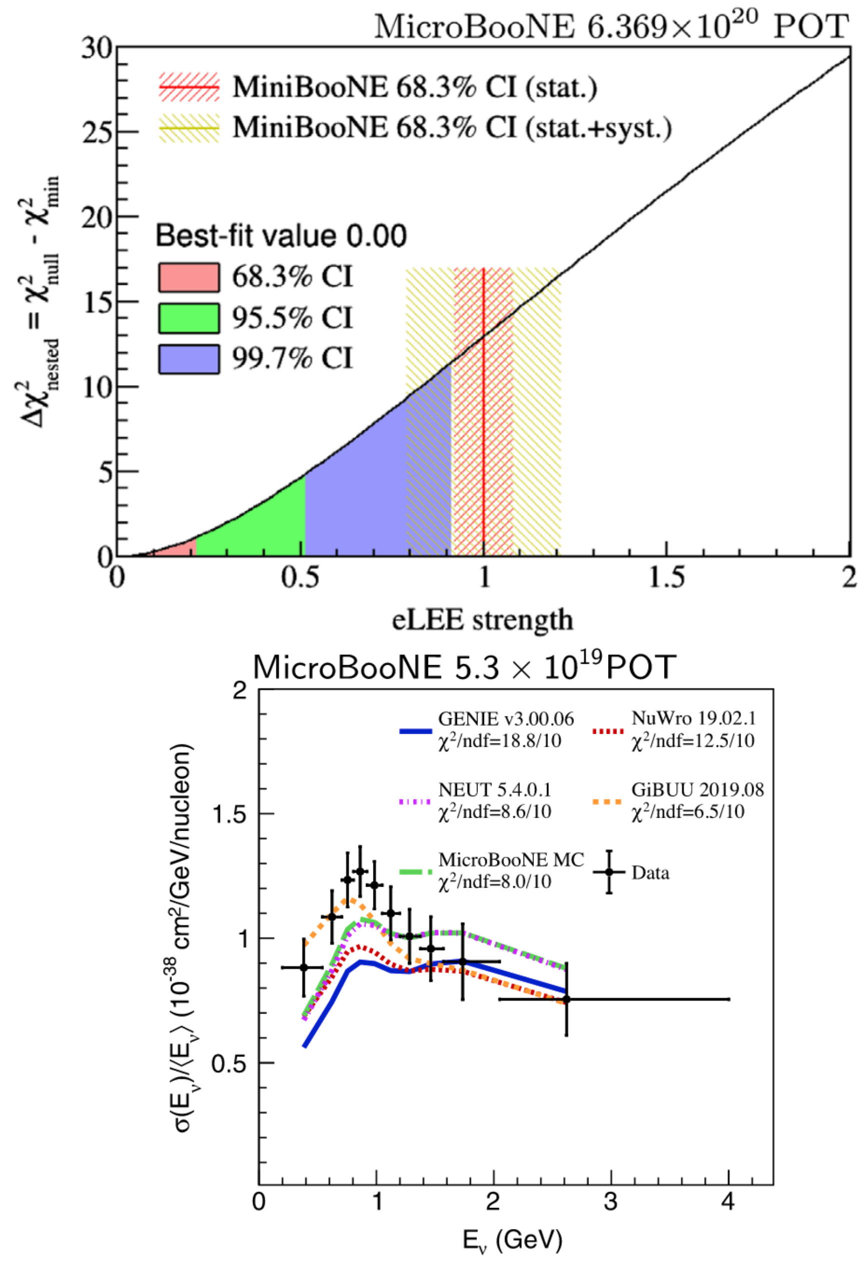
TPC simulation noise filtering signal processing	3D imaging clustering charge-light matching	3D trajectory & dQ/dx fitting cosmic muon tagger	multi-track fitting DL-3D vertexing particle identification	model validation statistical analysis data analysis









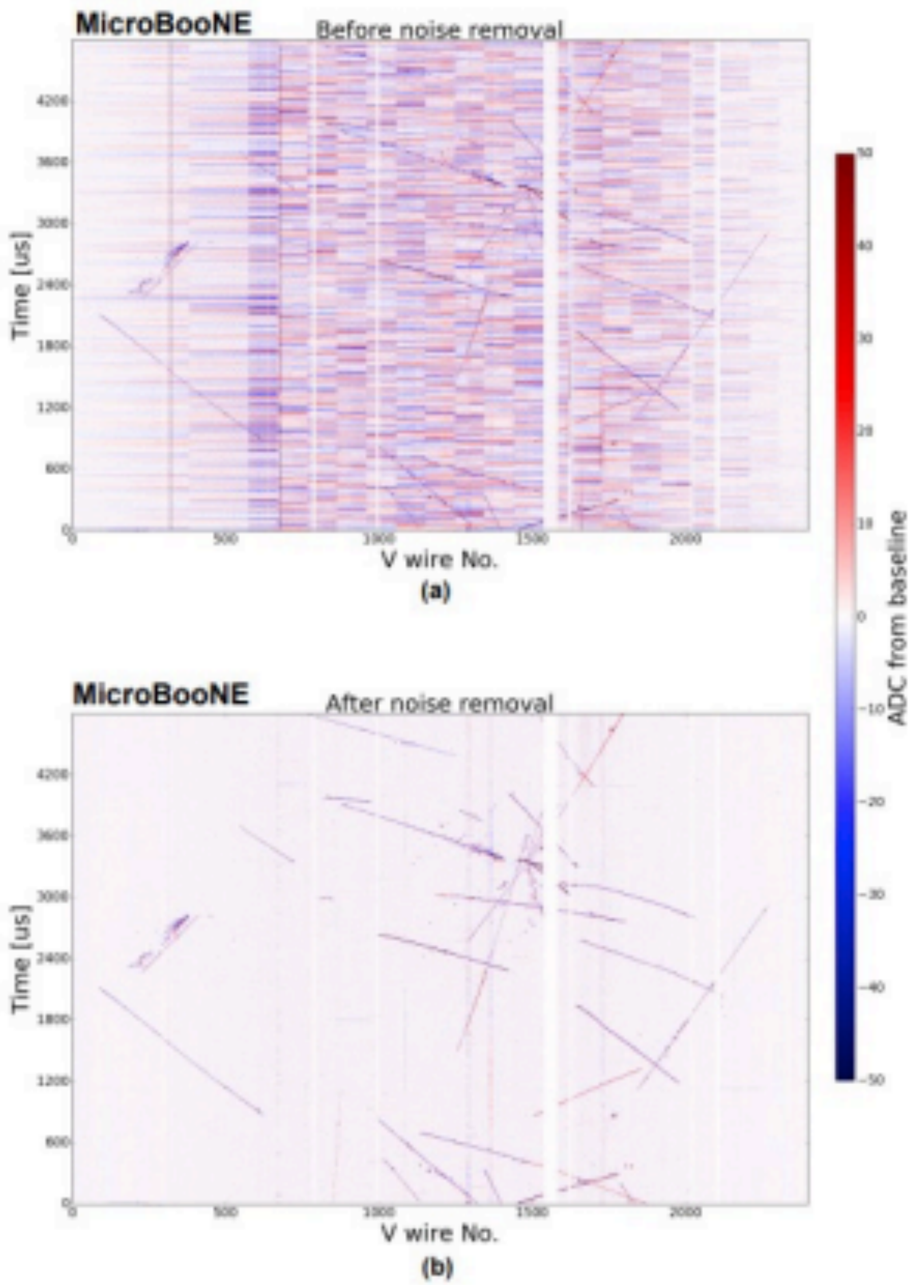


Wire-Cell is a collection of software tools for LArTPC that processes from signal processing to event reconstruction and physics analysis, made a huge success in MicroBooNE

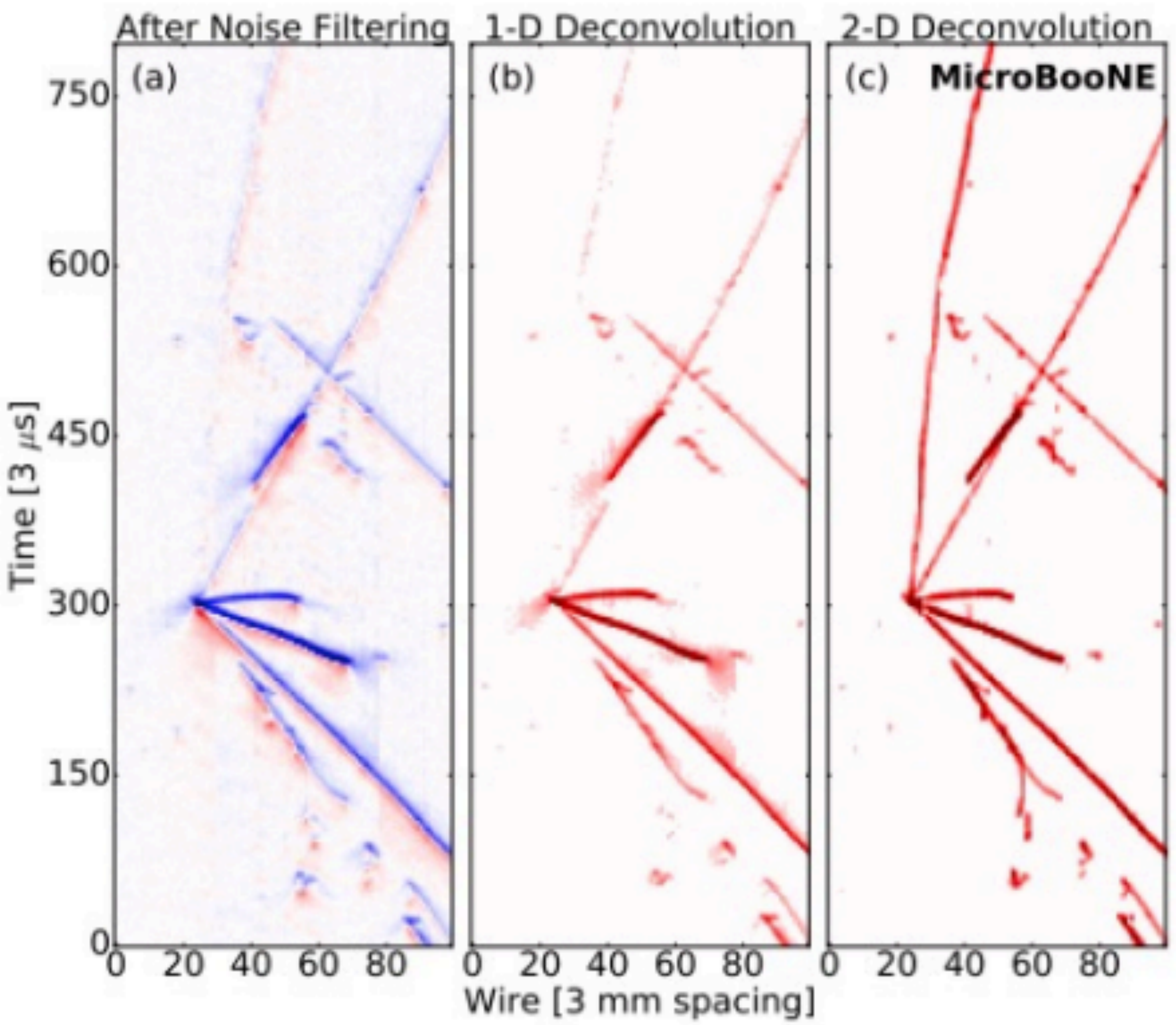
Noise filtering & Signal processing (WCP example)

Chao Zhang

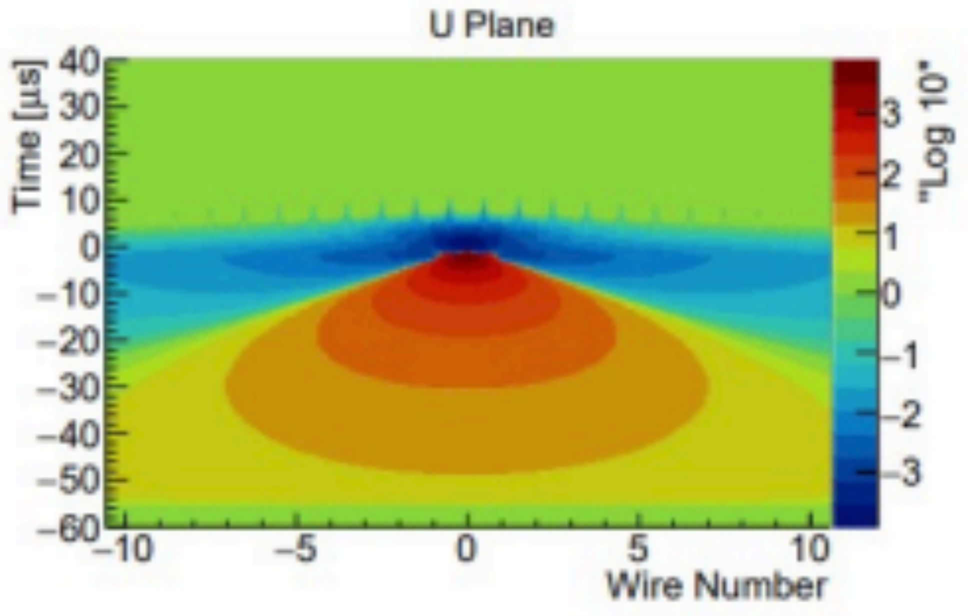
Example event from MicroBooNE before and after noise filtering
JINST 12, P08003 (2017)



Example event from MicroBooNE before and after signal processing
JINST 13, P07006 (2018)

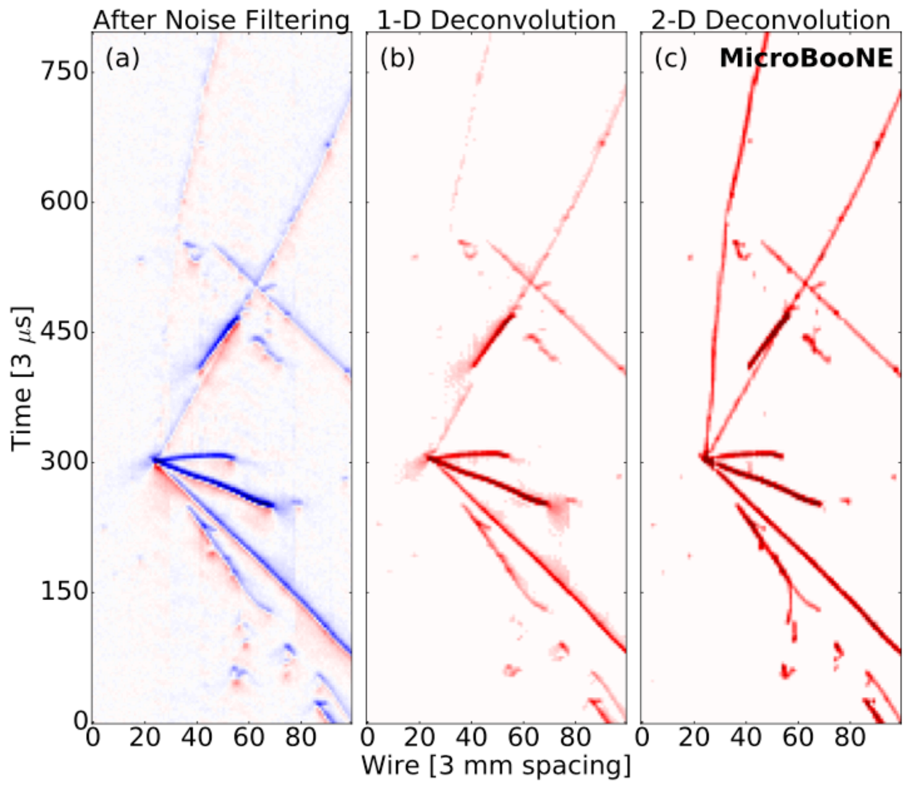


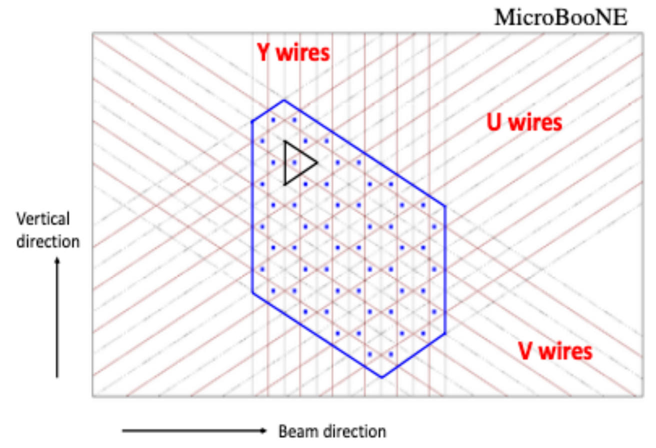
2D field response taking into account long range induction effect up to ±10 wires

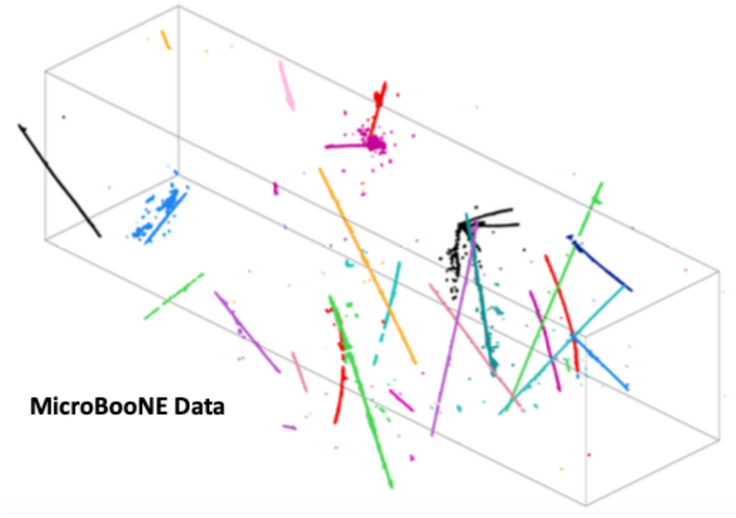


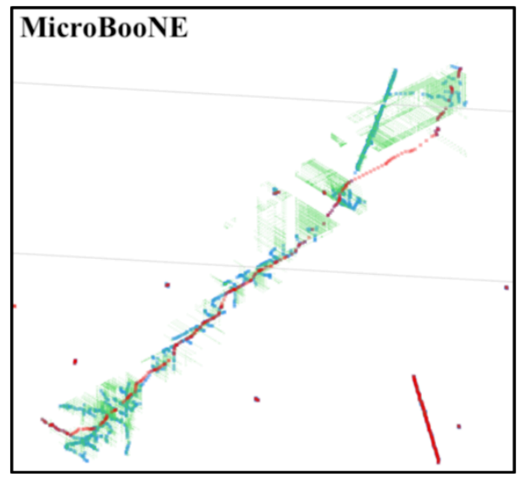
Wire-Cell-Toolkit (WCT)

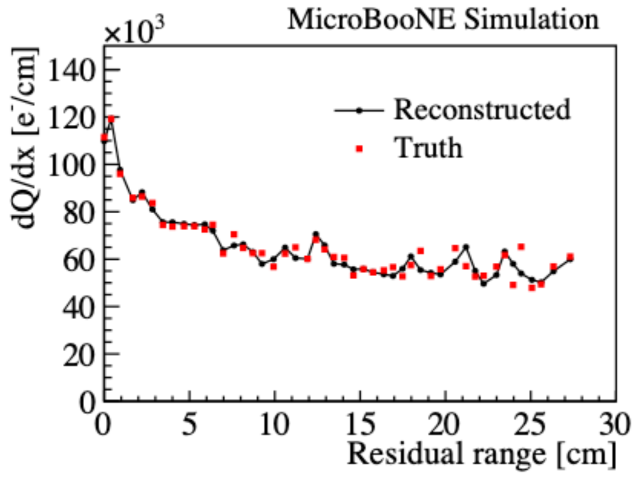
TPC simulation noise filtering signal processing	3D imaging clustering charge-light matching	3D trajectory & dQ/dx fitting cosmic muon tagger	multi-track fitting DL-3D vertexing particle identification	model validation statistical analysis data analysis

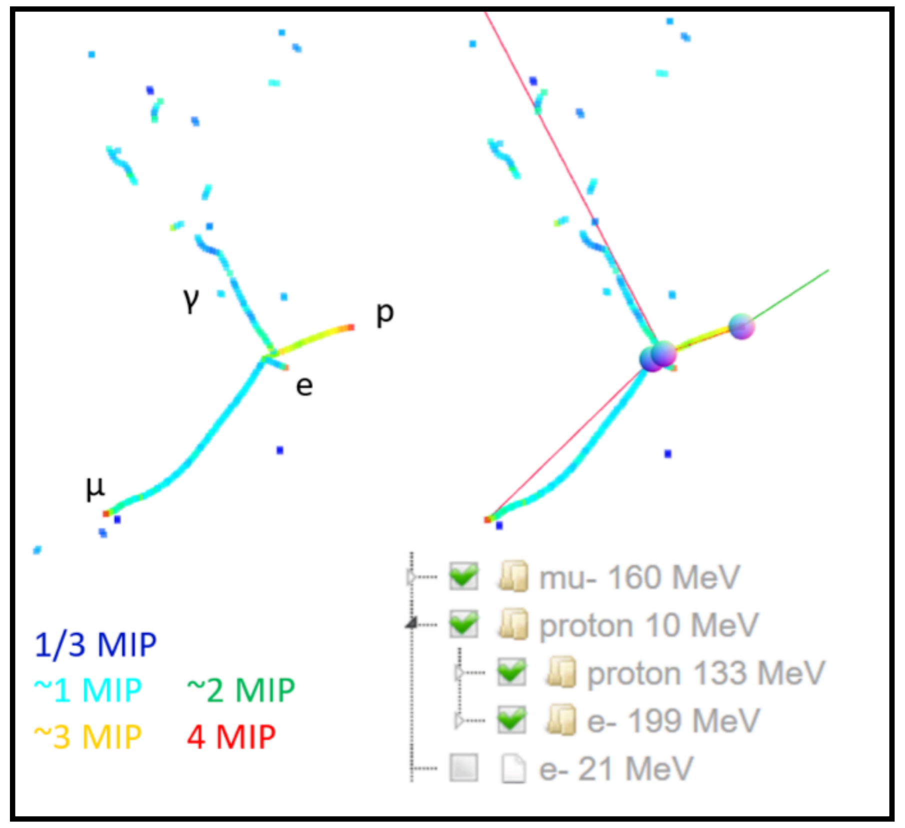


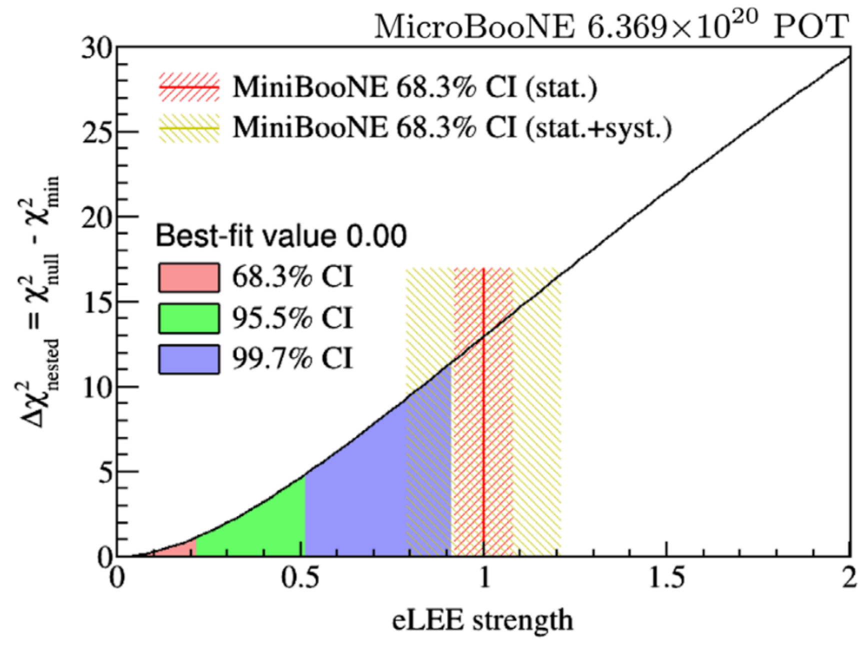


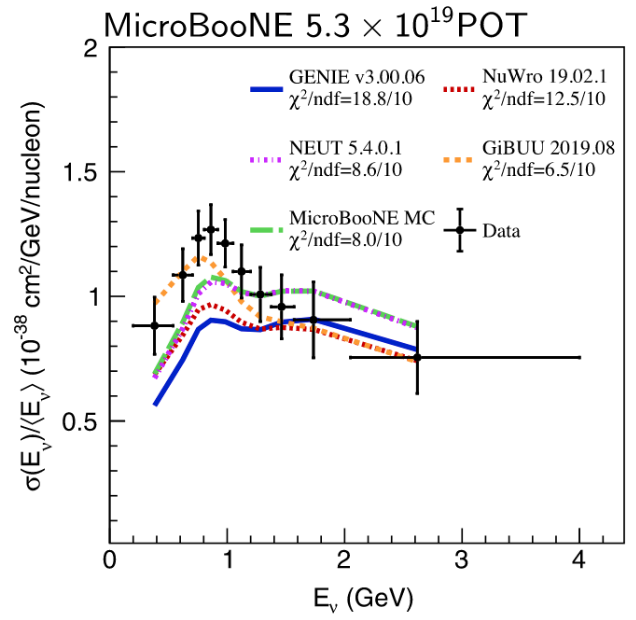










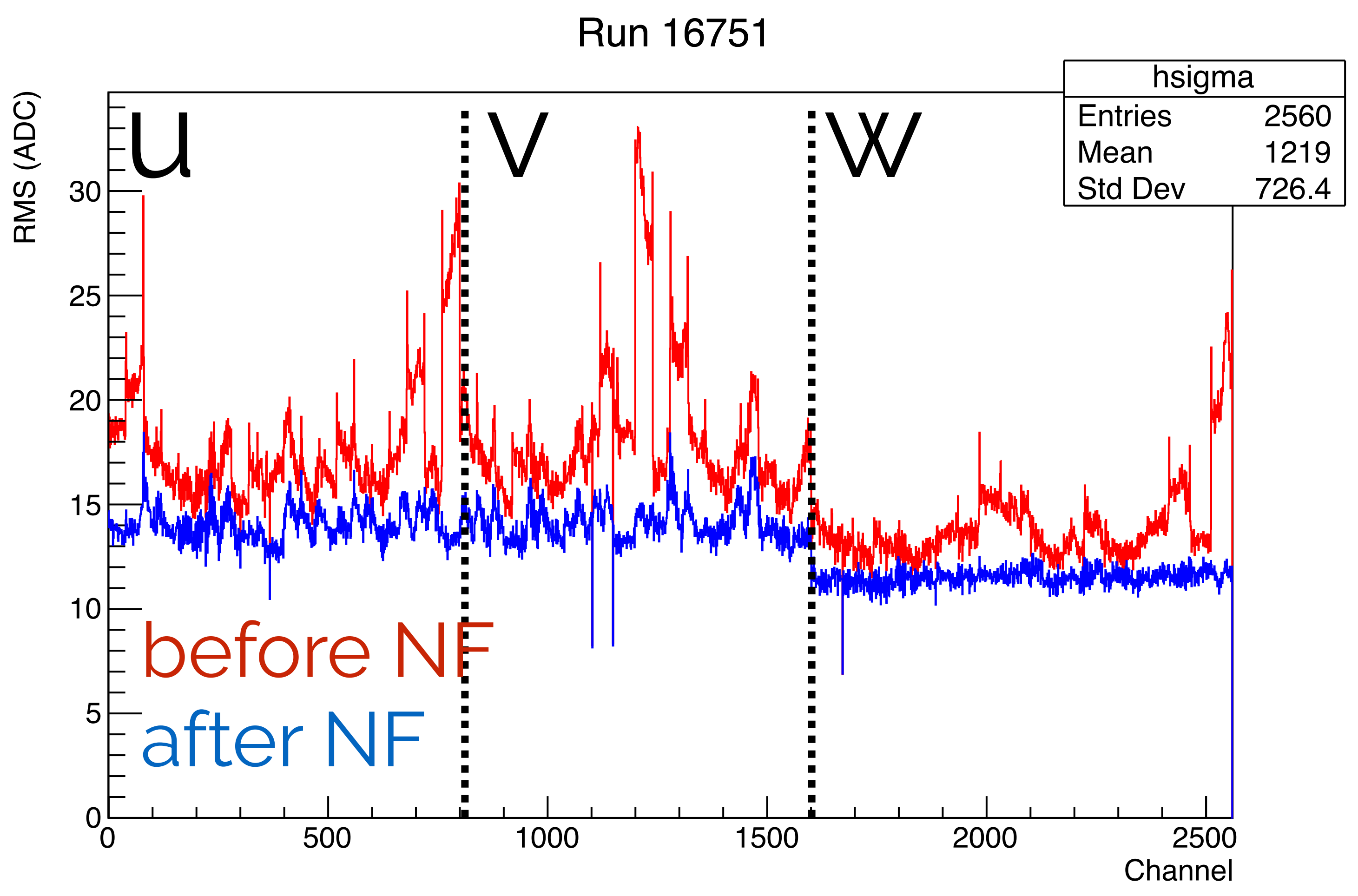


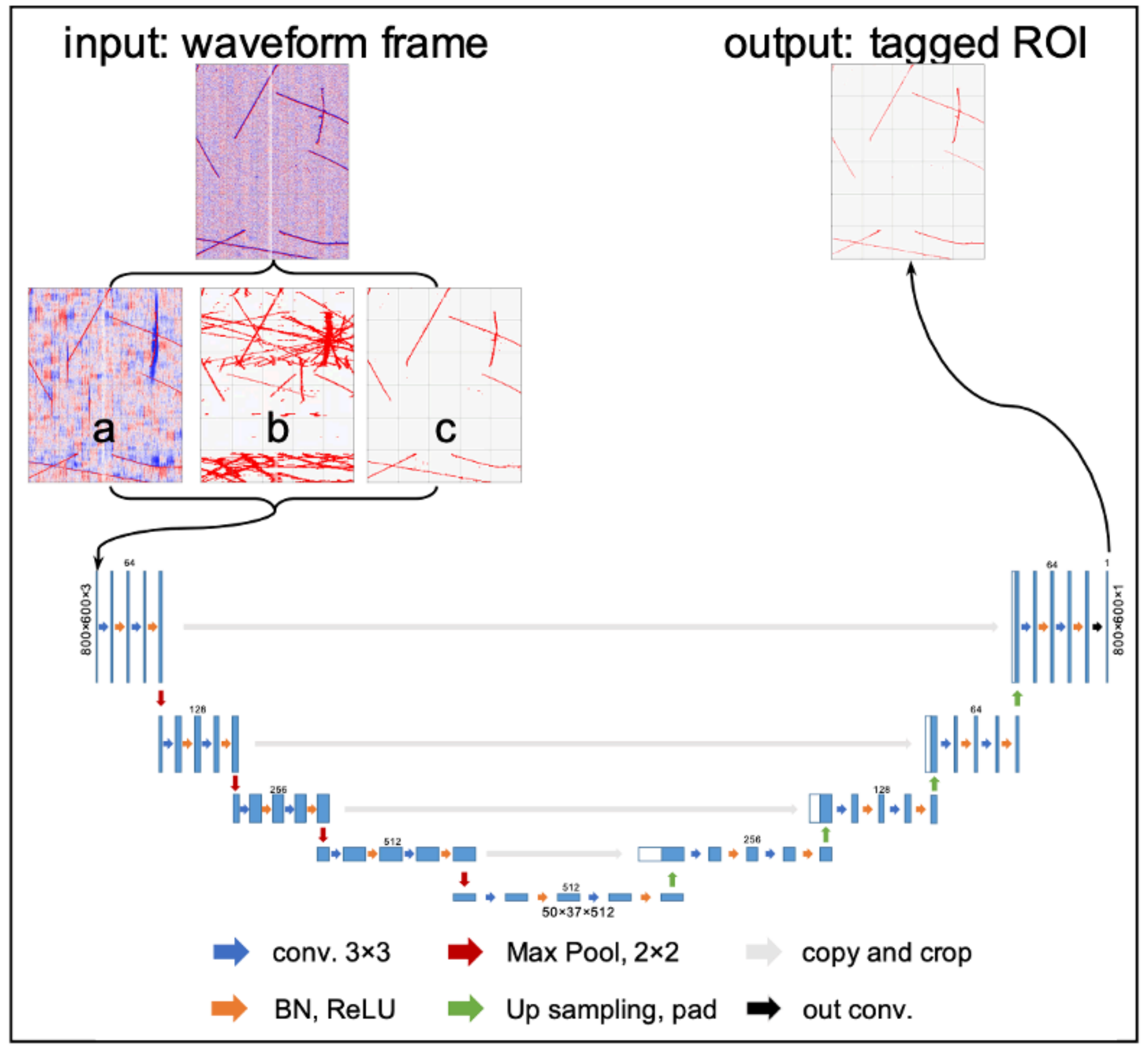
currently making progress in "porting" the WCP into more generic WCT for other LArTPC experiments such as SBND, ICARUS, ProtoDUNEs, and DUNE

Noise filtering & Signal processing (WCT example)

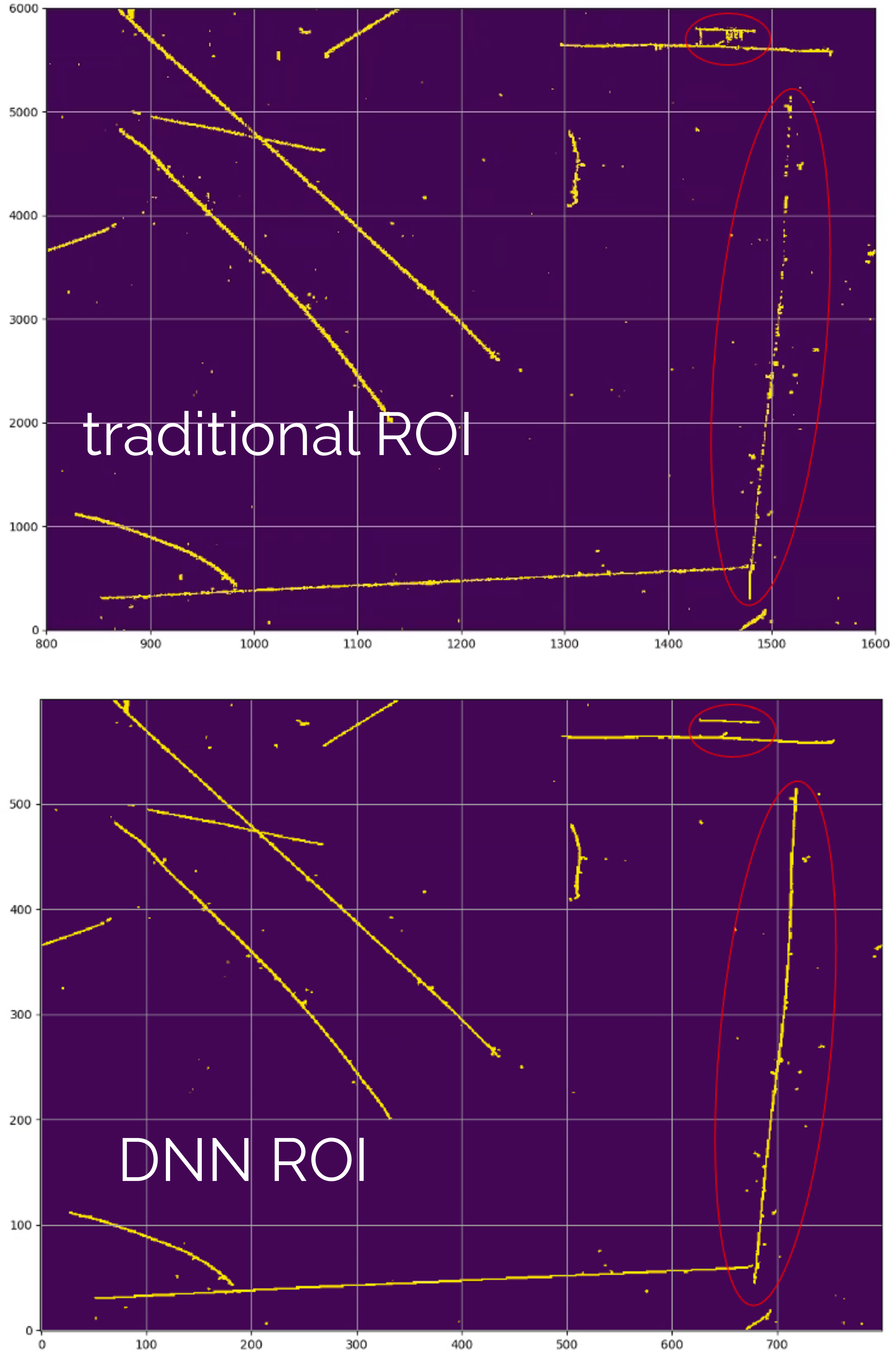
- upstream part of WC is implemented/used in SBN and PD
- porting work of downstream part of WC is being carried out as we speak
- further improvements with AI/ML tools are developing

PD-HD noise filtering





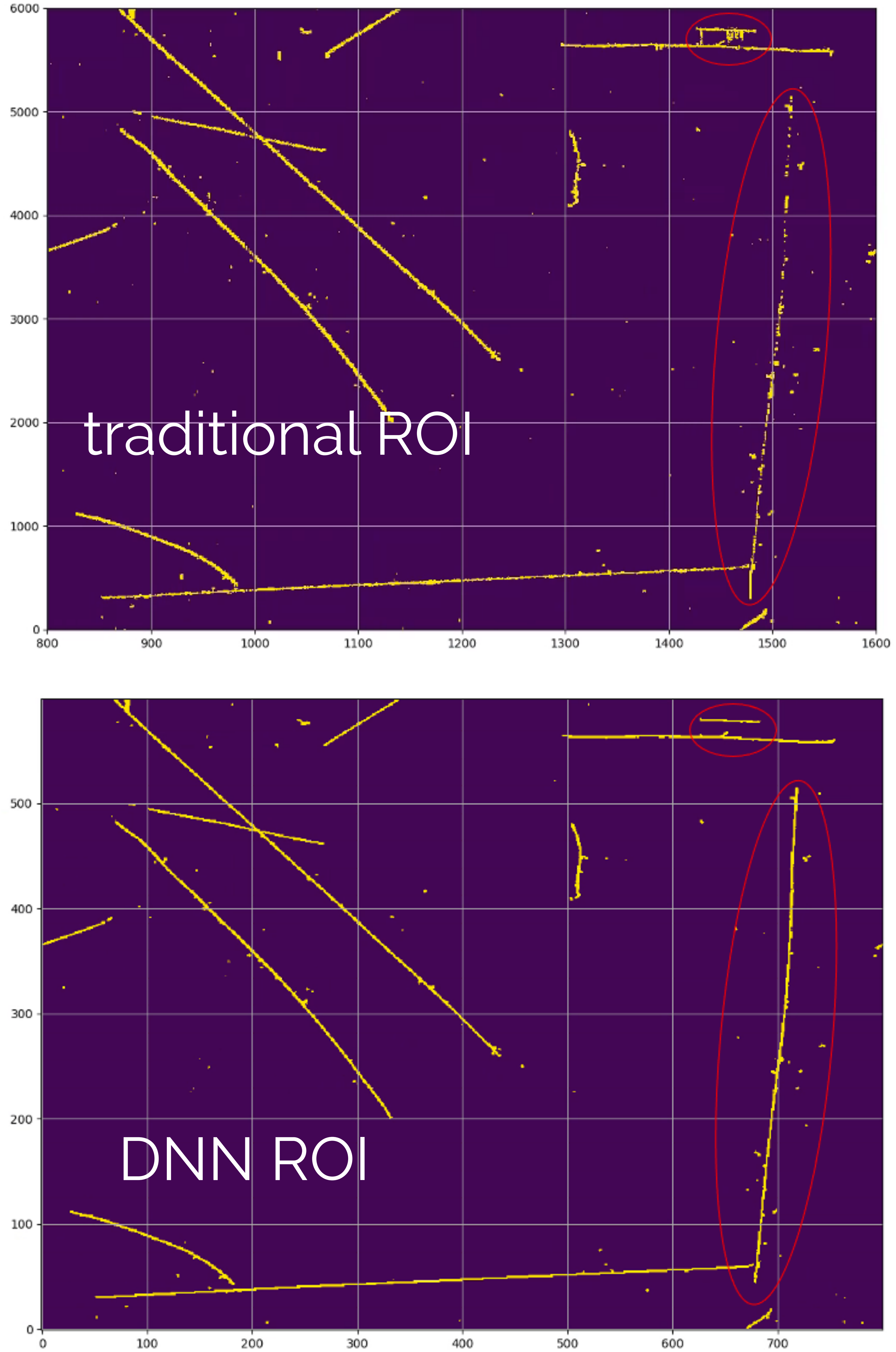
PD-SP data



Software: Wire-Cell status & plan

- upstream part of WC is already implemented/used in SBN and PD
- porting work is being carried out as we speak
- improvements with AI/ML tools are developing

PD-SP data: Run 5145 subrun 1 event 26945, v plane



H. Yu, CPAD 2021

Brett Viren

- BNL is leading noise filtering, signal processing and detector simulation for ProtoDUNE/DUNE with Wire-Cell

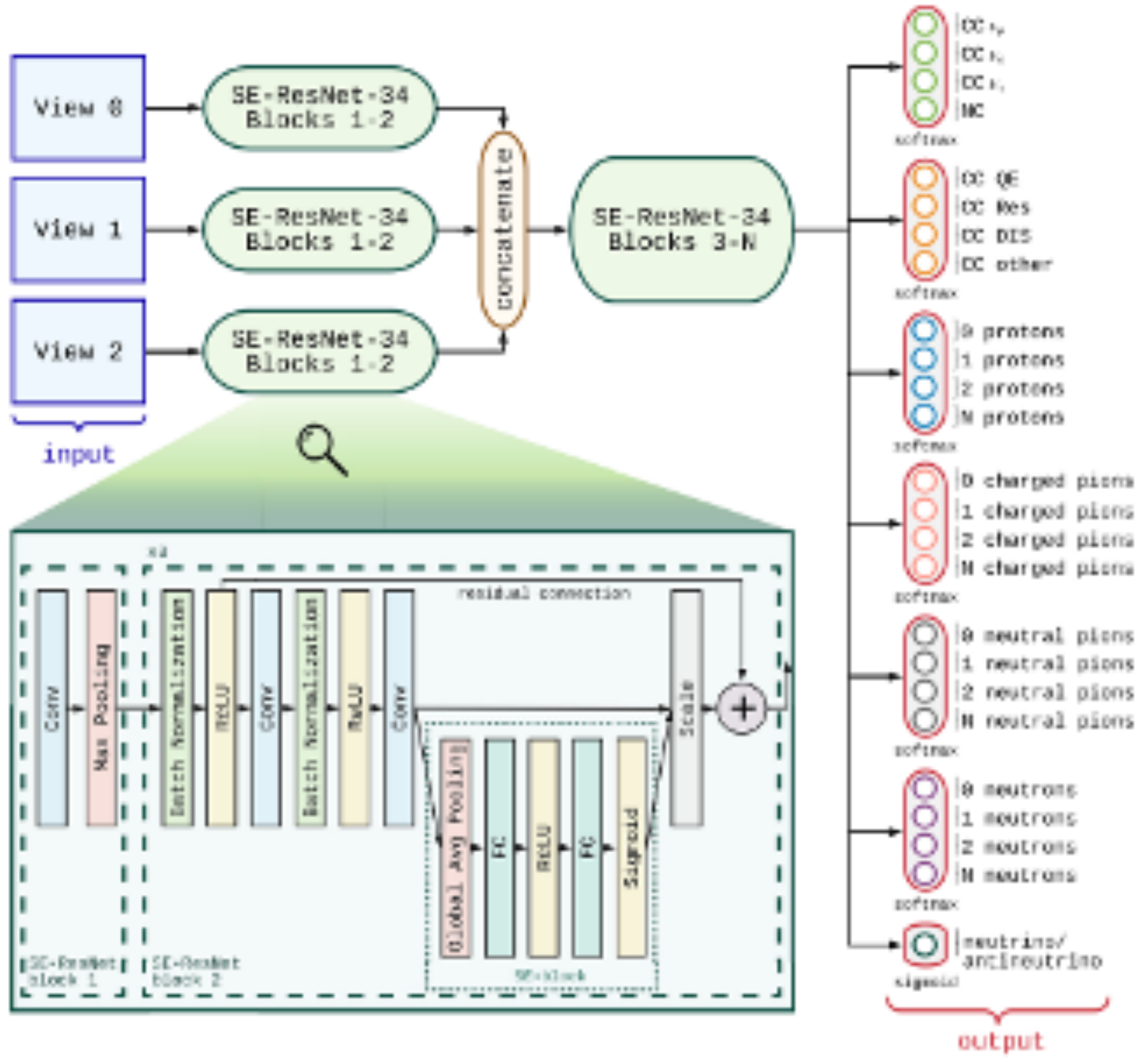
- with WCT available, BNL aims to actively engaged in oscillation analysis, cross section measurements, low energy physics
  - ProtoDUNE and SBN experiments are providing valuable testing ground

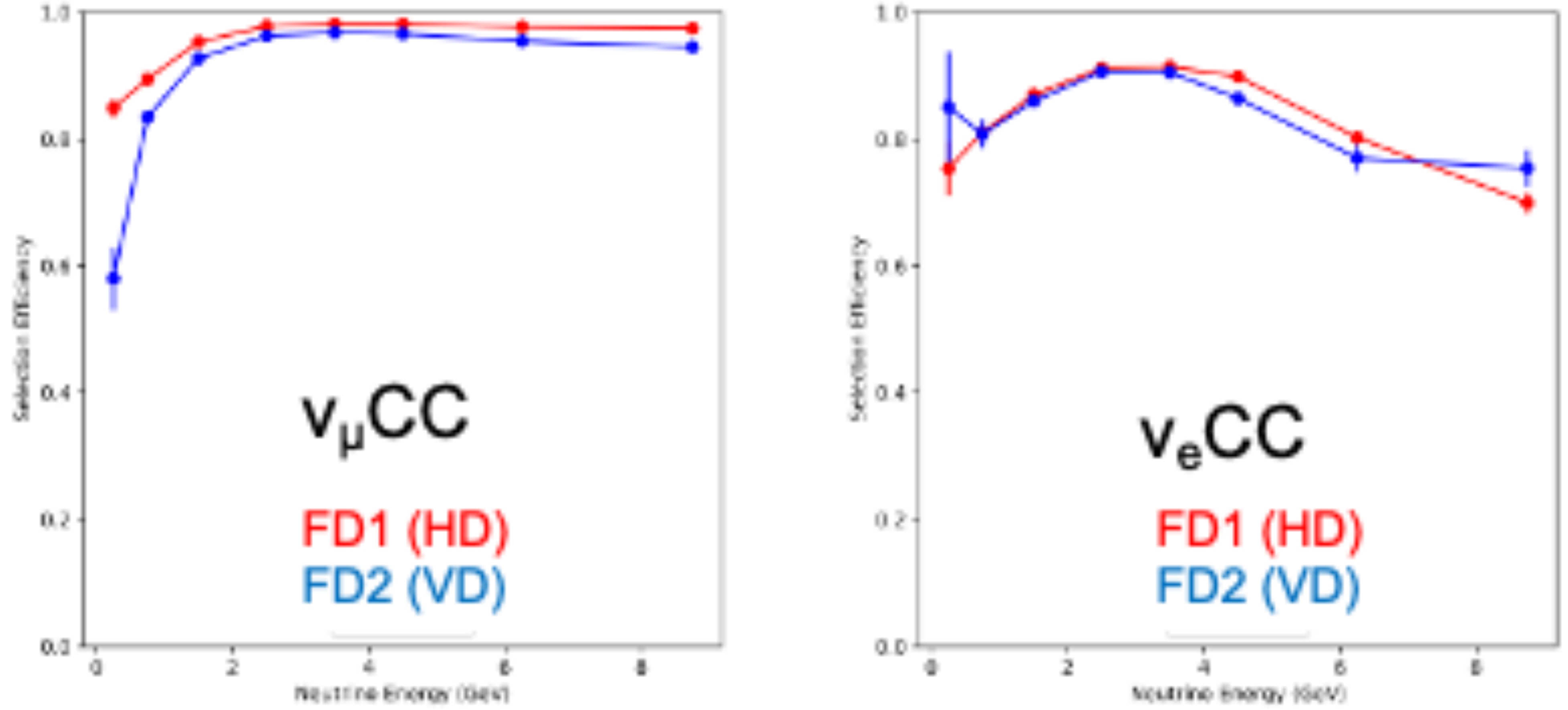
Longer Wire-Cell historical timeline

- 2015-03-15 First commit to BNLIF/wire-cell starting what will be known as the **prototype**.
- 2015-07-06 Wire-Cell **toolkit** starts new GitHub org/repo WireCell/wire-cell-toolkit.
- 2015-10-08 The wire-cell command line program starts.
- 2015-10-14 First JsonCPP for configuration objects.
- 2015-11-05 WireCell/wire-cell-tbb starts MT data-flow graph engine.
- 2015-12-15 Modern INode design started.
- 2016-03-02 WireCell/wire-cell-cfg Jsonnet configuration starts.
- 2016-04-29 WireCell/wire-cell-sigproc starting with noise filtering.
- 2016-12-20 Initial larwirecell module for noise filtering.
- 2017-04-09 Introduction of Jsonnet as configuration langauge.
- 2017-06-27 Actual OmnibusSigProc signal processing starts.
- 2017-06-28 wire-cell CLI factored out to WireCell::Main for
- 2017-07-05 Modern larwirecel integration design.
- 2018-03-05 WireCell/wire-cell-pgraph starts ST, low mem DFP graph engine
- 2018-09-20 WireCell/wire-cell-gen gets today's 2D signal simulation.
- 2018-10-15 The streaming Drifter in gen.
- 2019-01-07 WireCell/wire-cell-img starts with "time slicing".
- 2019-01-25 The "ray grid" 3D "tiling" method invented, added to img.
- 2019-02-11 Add ProtoDUNE-SP support to noise filtering.
- 2019-08-23 Join submodules into monorepo at WireCell/wire-cell-toolkit.
- 2019-11-15 wire-cell-toolkit/pytorch starts with DNNROI.
- 2020-02-28 wire-cell-toolkit/zio subpackage starts.
- 2022-03-10 start of post-tiling imaging porting from prototype.
- 2022-04-26 tar/zip files streams and custom Numpy I/O.
- 2022-09-29 start of imaging sampling to point cloud.
- 2024-03-19 port of prototype clustering.

CVN for DUNE-VD

- DUNE Convolutional Visual Network developed for DUNE FD-HD for neutrino flavor tagging, establishing TDR sensivity
  - ResNet-based architecture with multiple wire-plane image inputs
- BNL implemented for DUNE FD-VD to validate & optimize detector design



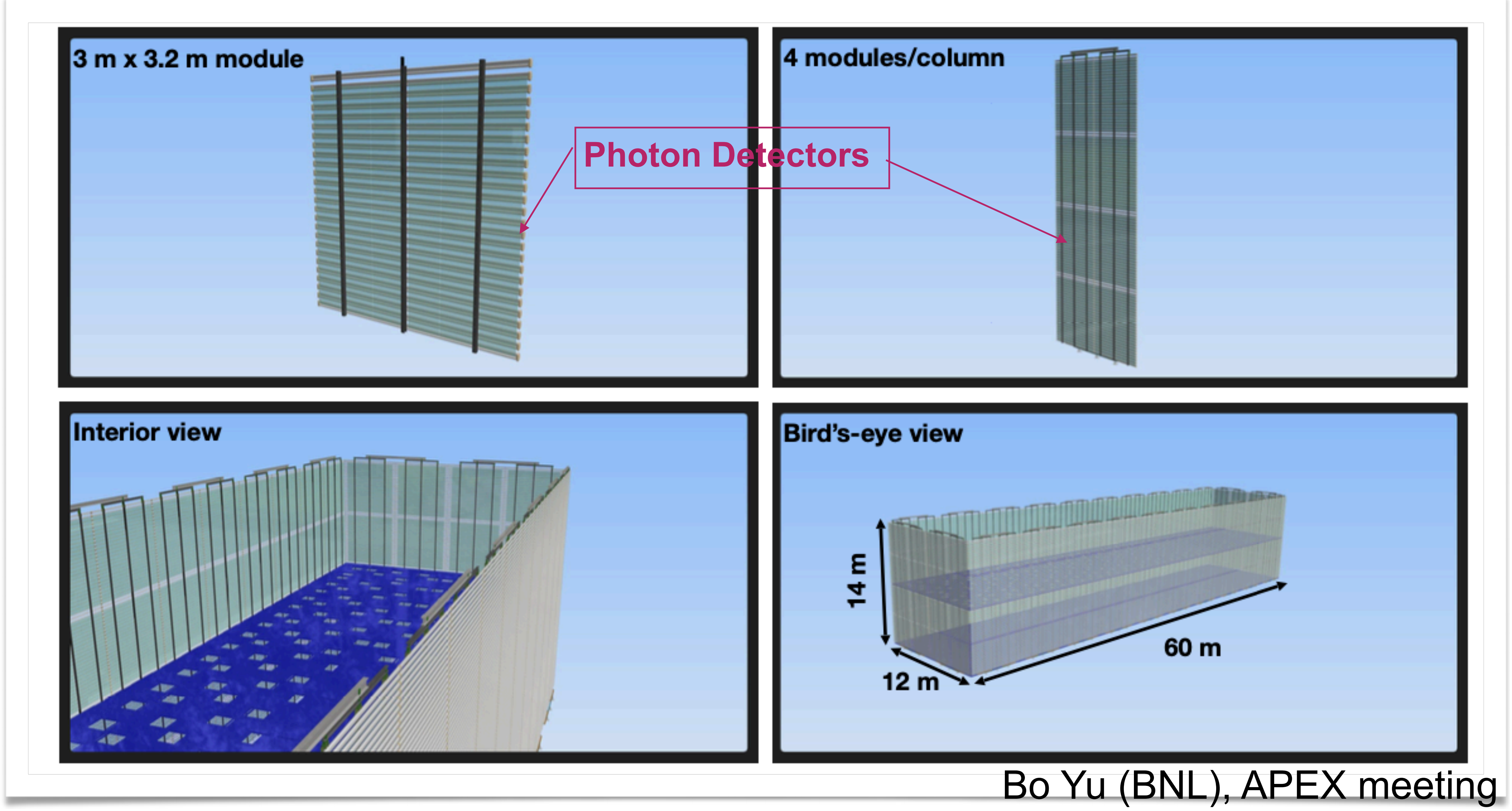


DUNE FD Phase II

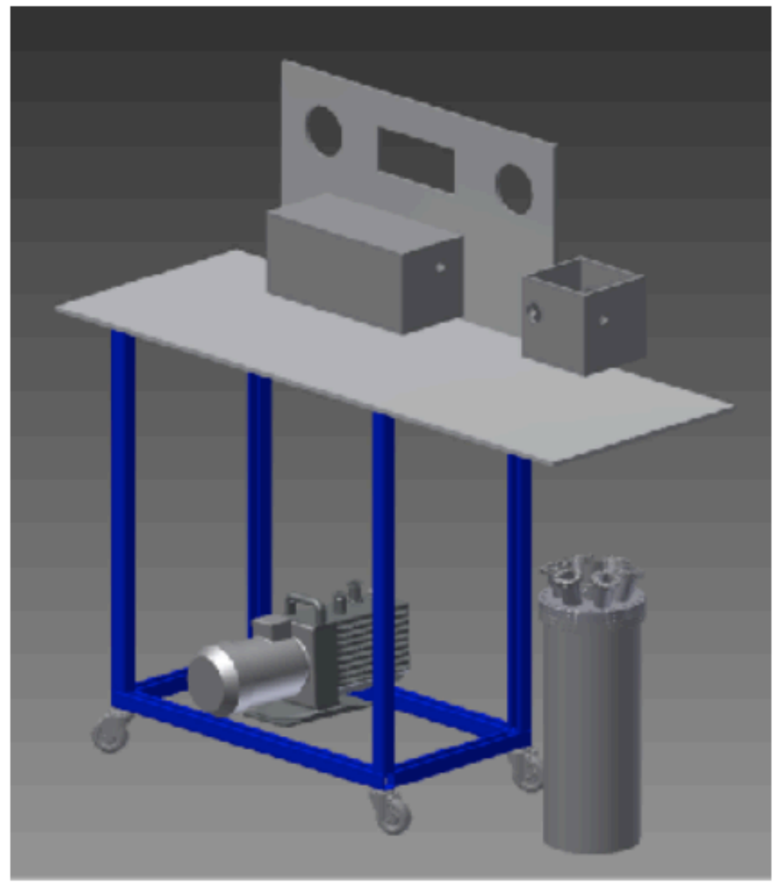
Yichen Li

- DUNE Phase II will add two extra FD modules
- leading design for FD3 is VD with enhanced photon detection system: APEX
- this will open a new door for improved GeV physics as well as rarely-explored-MeV physics with light calorimetry
- BNL is actively engaged in APEX design and development
- exploring R&D opportunities to optimize wavelength shifter coating for DUNE FD3 photon detection system

Proposed DUNE Phase-II FD3 Design



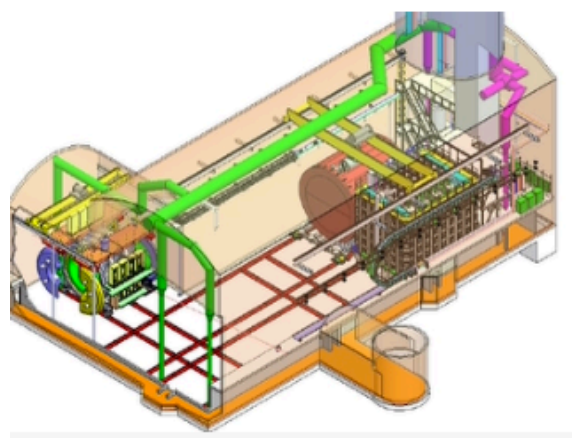
Bo Yu (BNL), APEX meeting



Summary

- BNL is driving progress on all fronts of DUNE
  - installation and commissioning FD-VD and FD-HD at SURF
  - production WC testing and final validation at CERN
  - advancing Wire-Cell and LArTPC reconstruction and computation tools

DUNE construction: Phase II



- Two additional FD modules
- Beamline upgrade to >2MW (ACE-MIRT)
- More capable Near Detector (ND-GAr)

P5 report endorses FD3, ACE-MIRT, and MCND in the next decade, and R&D toward FD4

Recommendation 2: Construct a portfolio of major projects that collectively study nearly all fundamental constituents of our universe and their interactions, as well as how those interactions determine both the cosmic past and future.

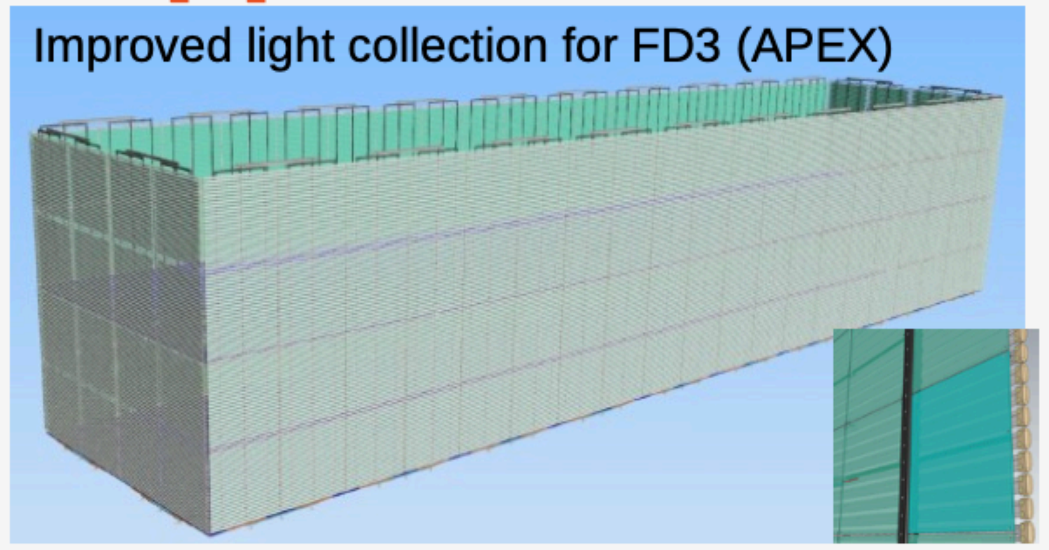
b. A re-envisioned second phase of DUNE with an early implementation of an enhanced 2.1 MW beam—ACE-MIRT—a third far detector, and an upgraded near-detector complex as the definitive long-baseline neutrino oscillation experiment of its kind

Recommendation 4: Invest in a comprehensive initiative to develop the resources—theoretical, computational, and technological—essential to realizing our 20-year strategic vision. This includes an aggressive R&D program that, while

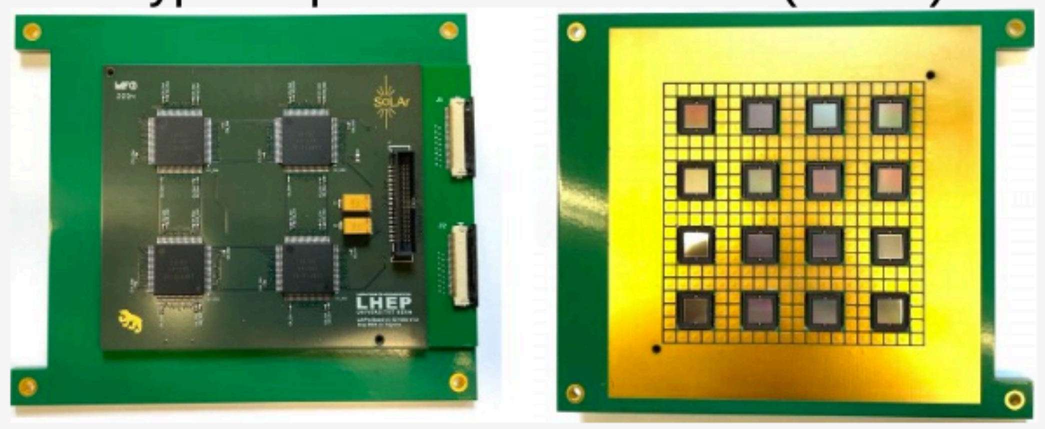
e. Conduct R&D efforts to define and enable new projects in the next decade, including detectors for an e^+e^- Higgs factory and 10 TeV pCM collider, Spec-S5, DUNE FD4, Mu2e-II, Advanced Muon Facility, and line intensity mapping

Phase II FD: additional mass + opportunities to expand physics reach

Improved light collection for FD3 (APEX)

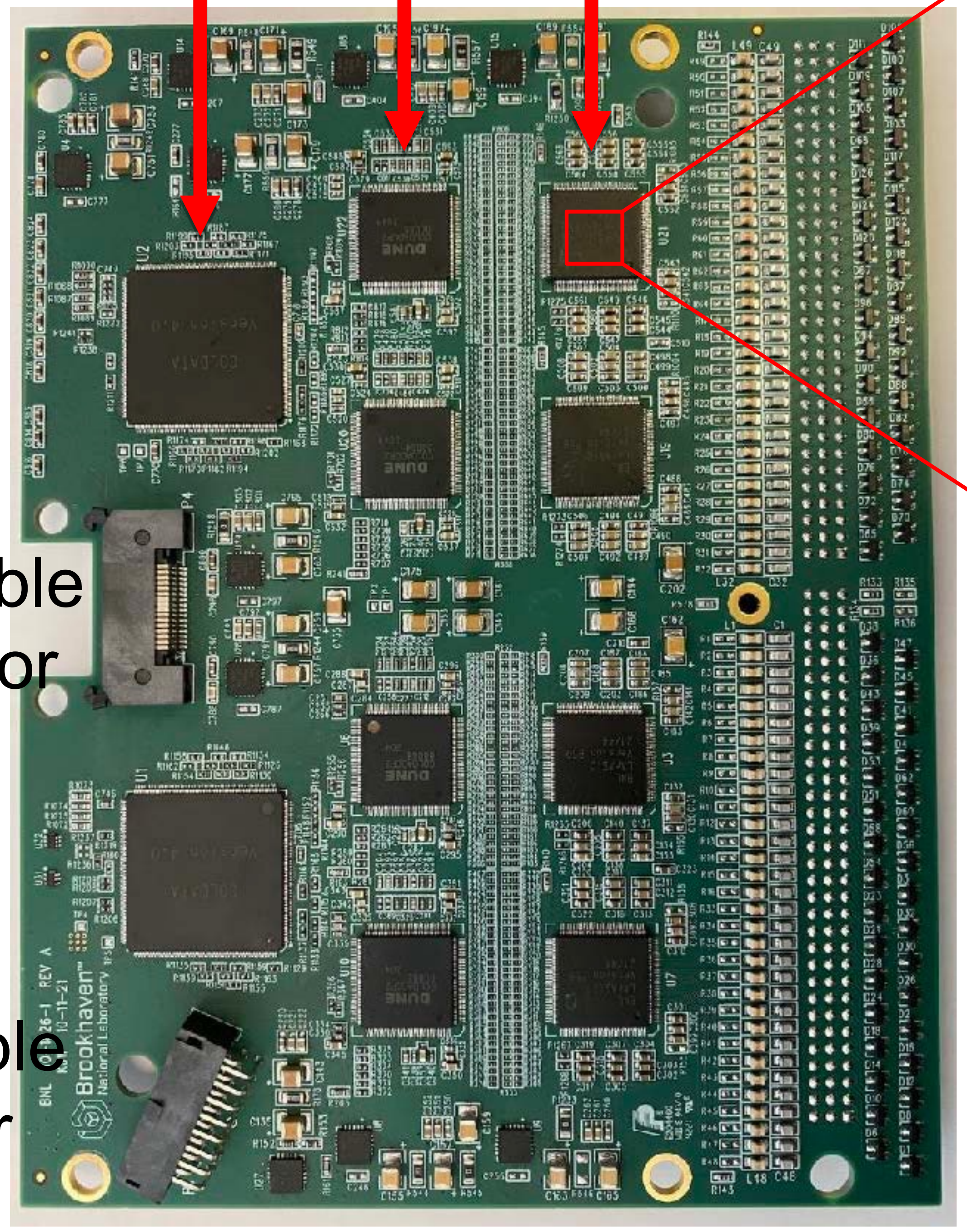


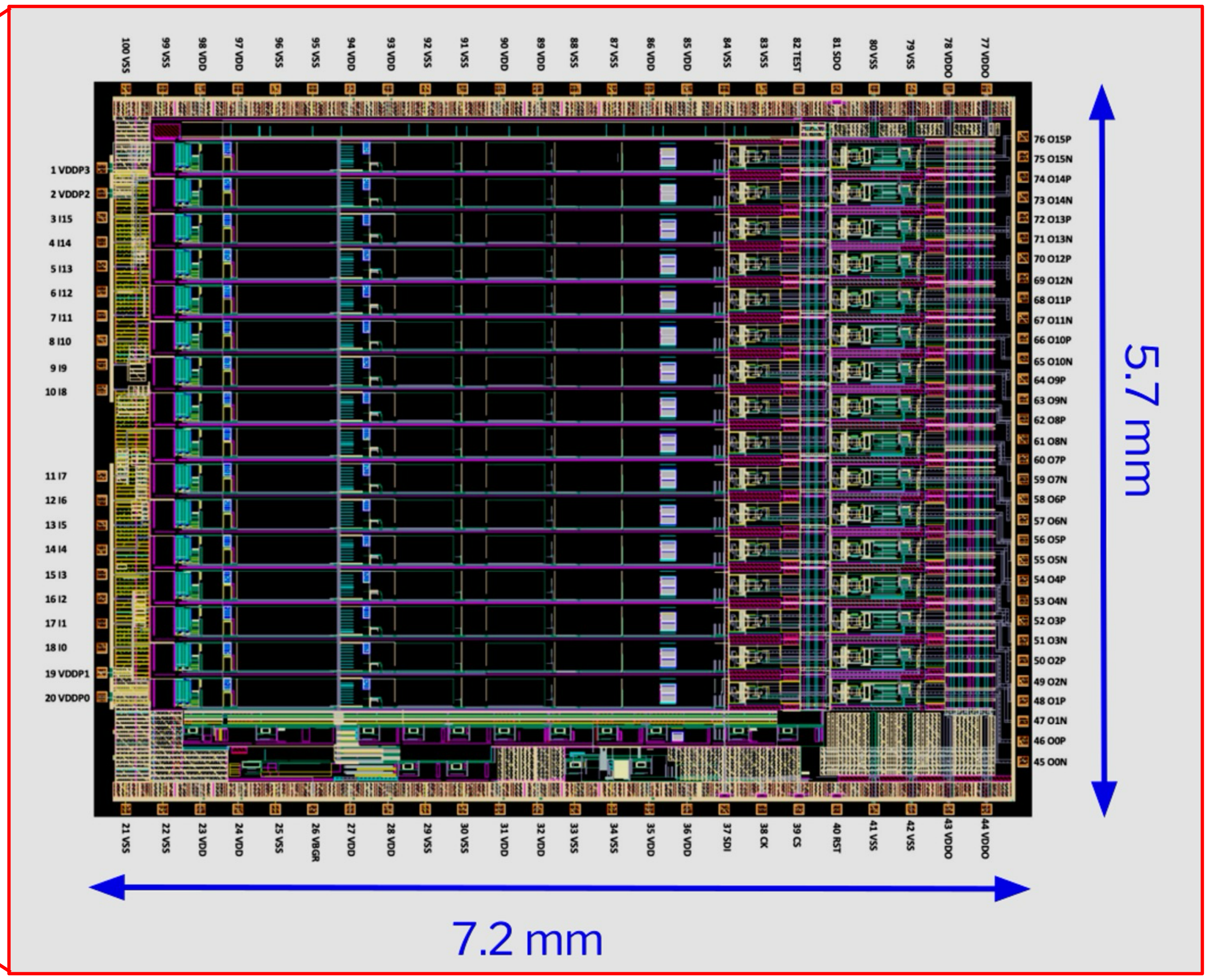
Prototype for possible FD4 readout (SoLAr)



- Vertical Drift module is the baseline design for Phase II FD modules
- Pursuing low-hanging improvements to light collection for FD3, including Aluminum Profiles with Embedded X-ARAPUCA, essentially integrating light detectors into field cage
- FD4 is the "Module of Opportunity", and more ambitious designs are being considered, including pixel readout, integrated charge-light readout, low background modules, and non-LAr technologies

Cryogenic Front End MotherBoard (FEMB)





- Each FEMB contains 3 ASICs:
  - 8 LArASIC amplifier/shapers
  - 8 ColdADC “2 MHz” ADCs
  - 2 COLDATA data concentrator and controllers

- Key specifications:
  - Low noise (<1000 e-)
  - High dynamic range (>500ke-)
  - ~2 MHz sampling frequency
  - At least 12 ADC bits

TPC ionization charge signal amplification, shaping, digitization, transmission.

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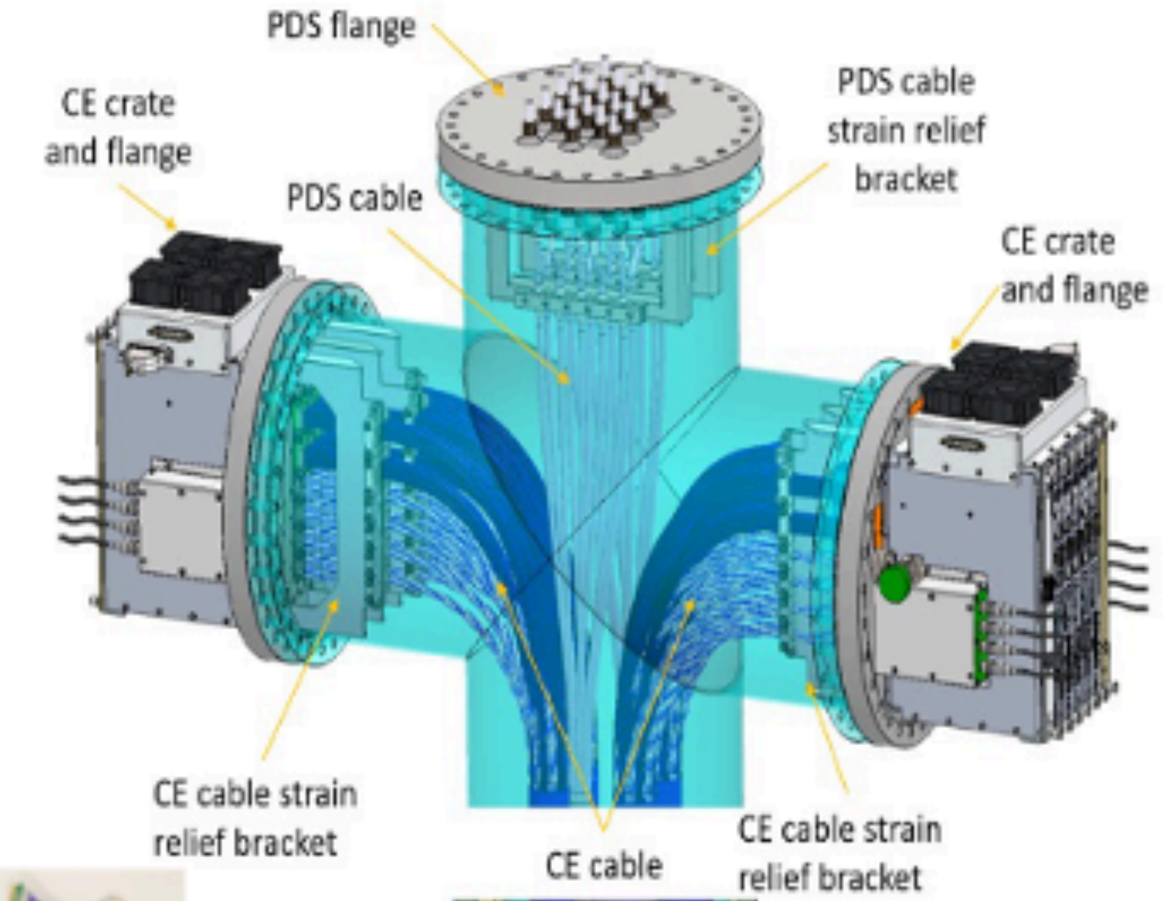
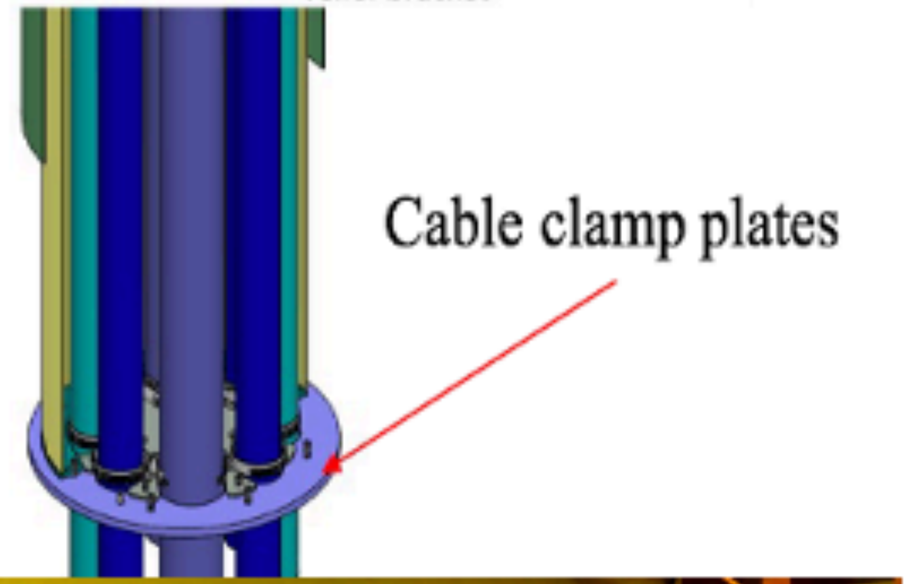
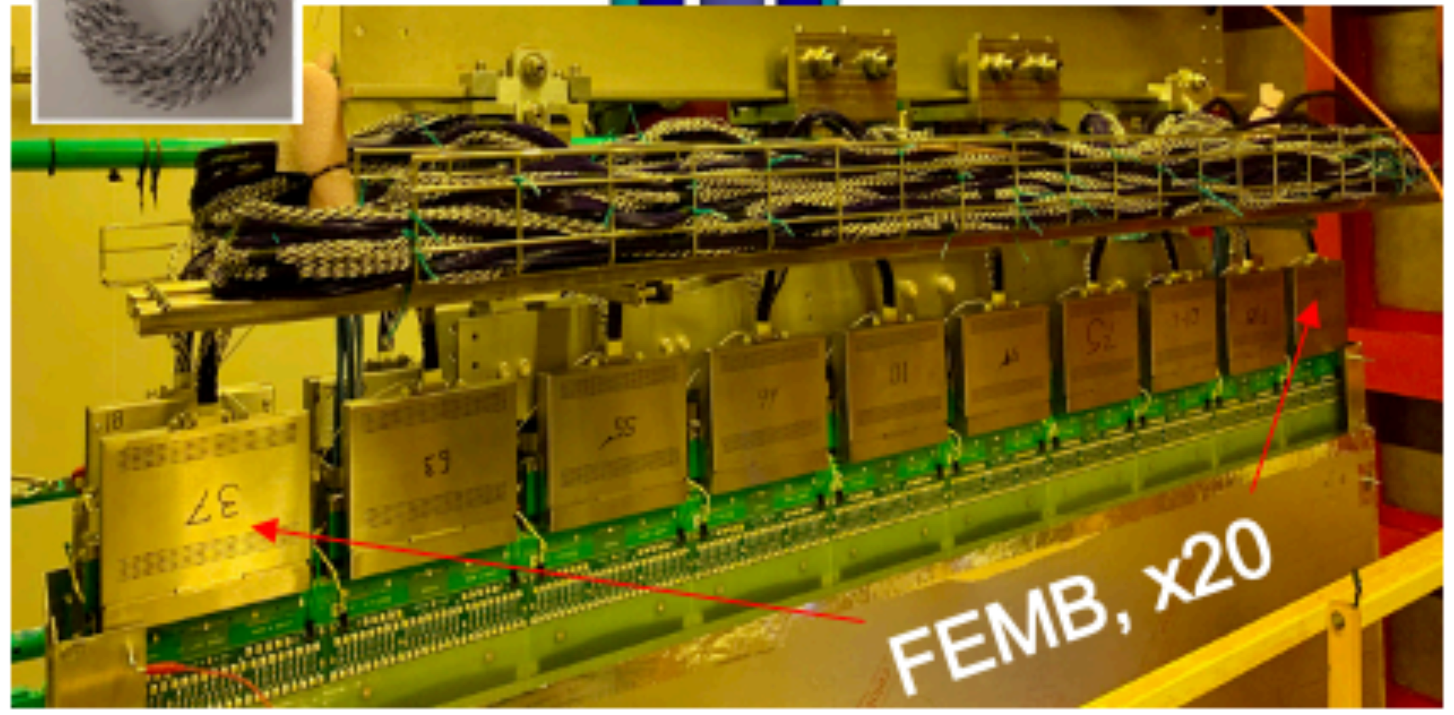
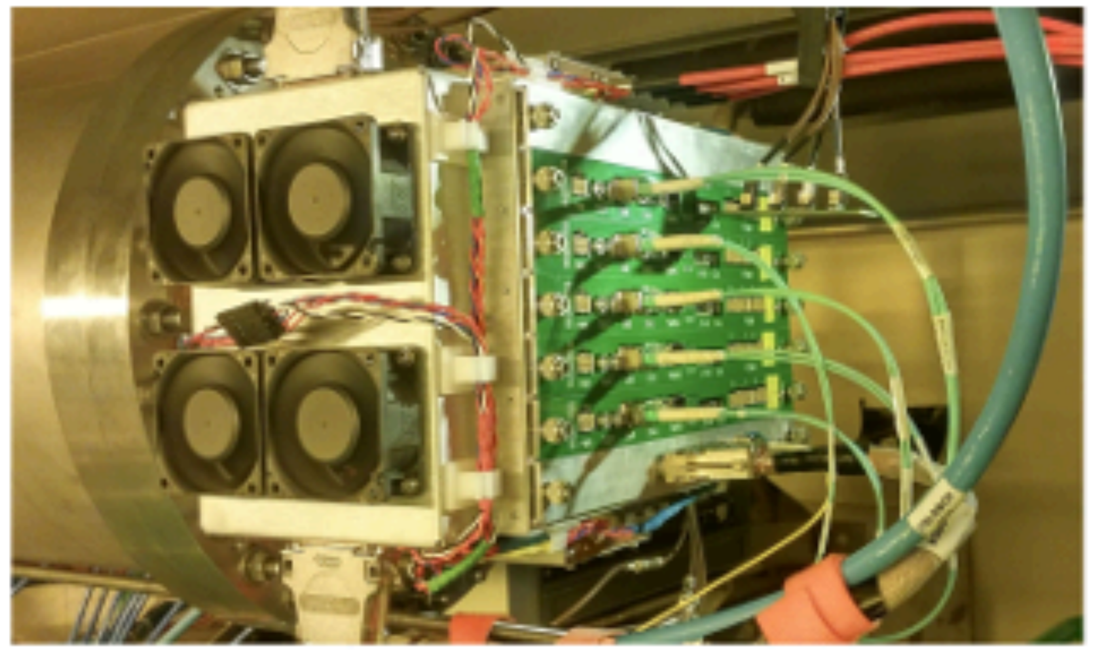
DUNE TPC detector Electronics + system Integration by BNL

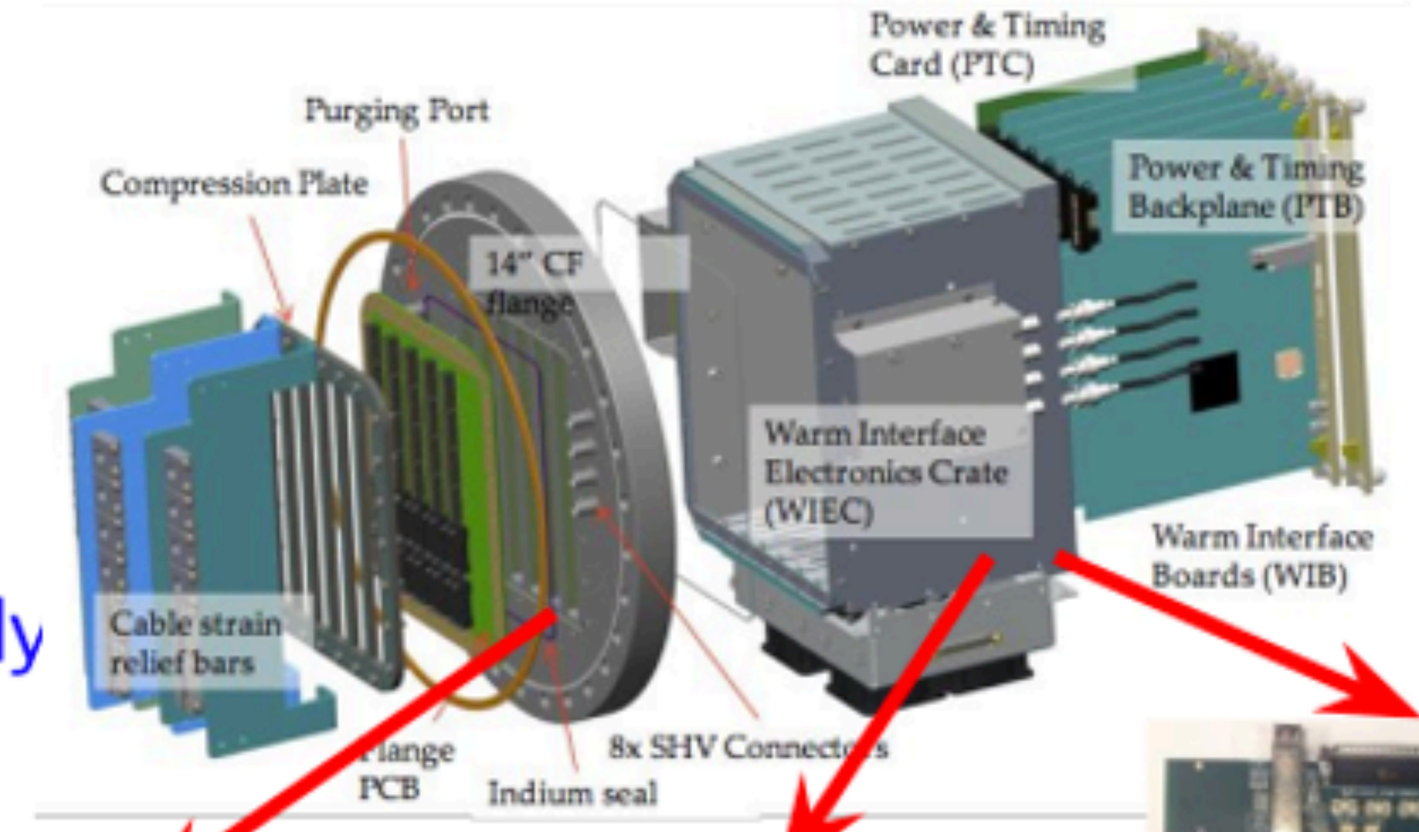


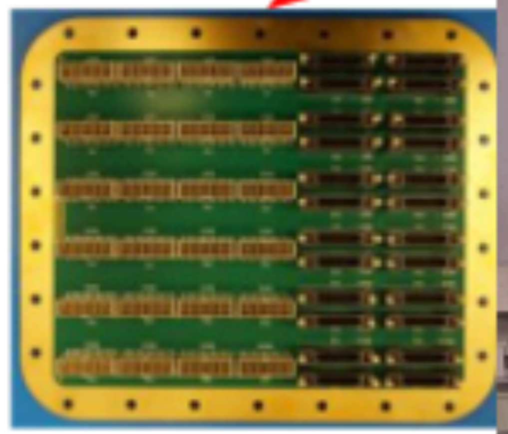


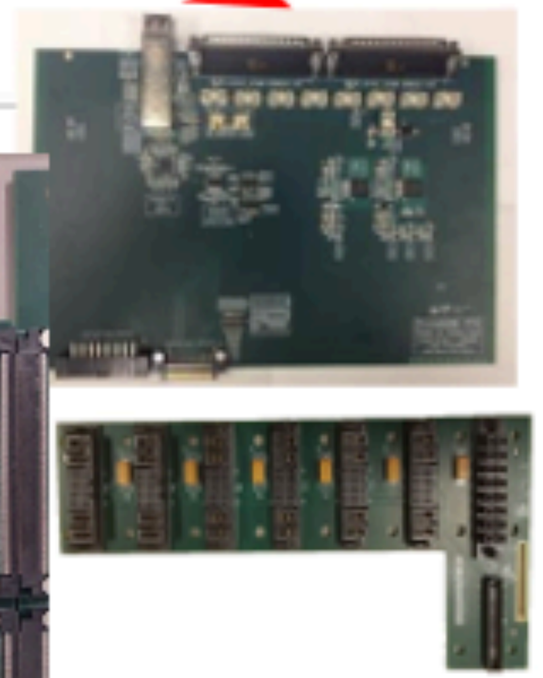




Signal Feed-through Assembly







Integral design:
Cold Electronics, cold power and data cables, cable strain relief, feedthrough flange board, warm electronics crate, power and timing card, warm interface board with fiber optic links to DAQ

Warm Interface Board (x5)
Xilinx Zynq UltraScale+ SOC FPGA
(includes ARM cores; can run Linux

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