µRwell technology for the IDEA detector

FUTURE CIRCULAR COLLIDER
Innovation Study

17 January 2024
Hong Kong

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on behalf of the RD_FCC collaboration
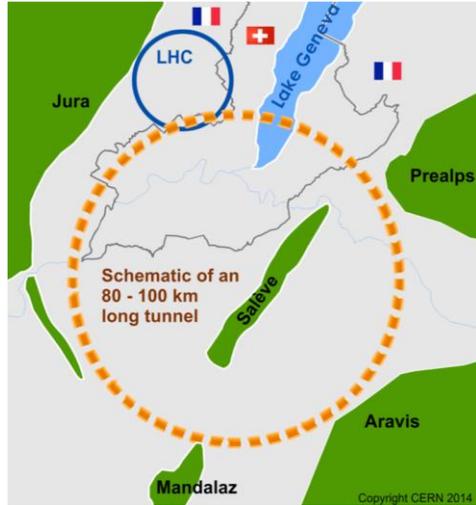
INFN
Istituto Nazionale di Fisica Nucleare

AGENDA

- IDEA detector concept
- µRwell technology
- Readout electronics
- Results from beam tests
- Technology transfer
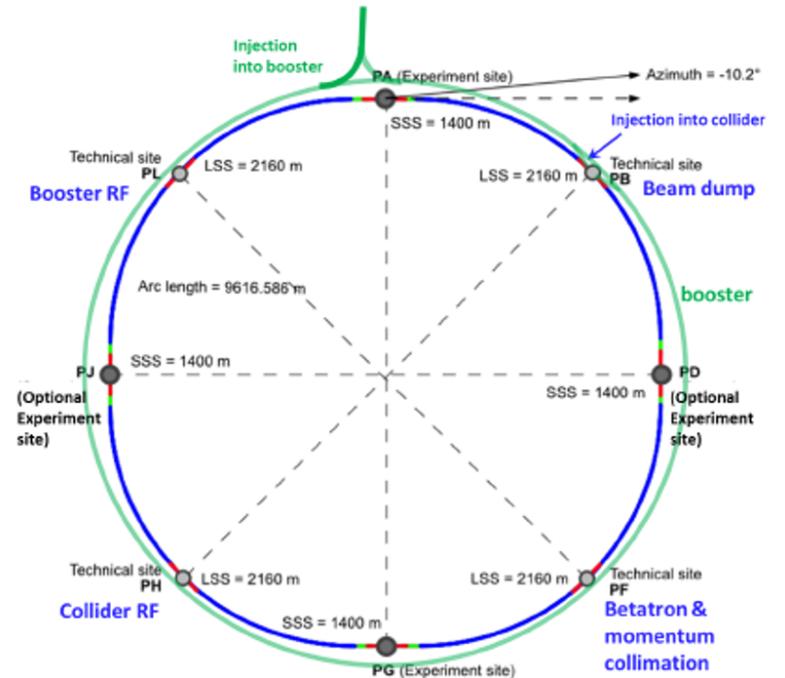- Status and future perspectives
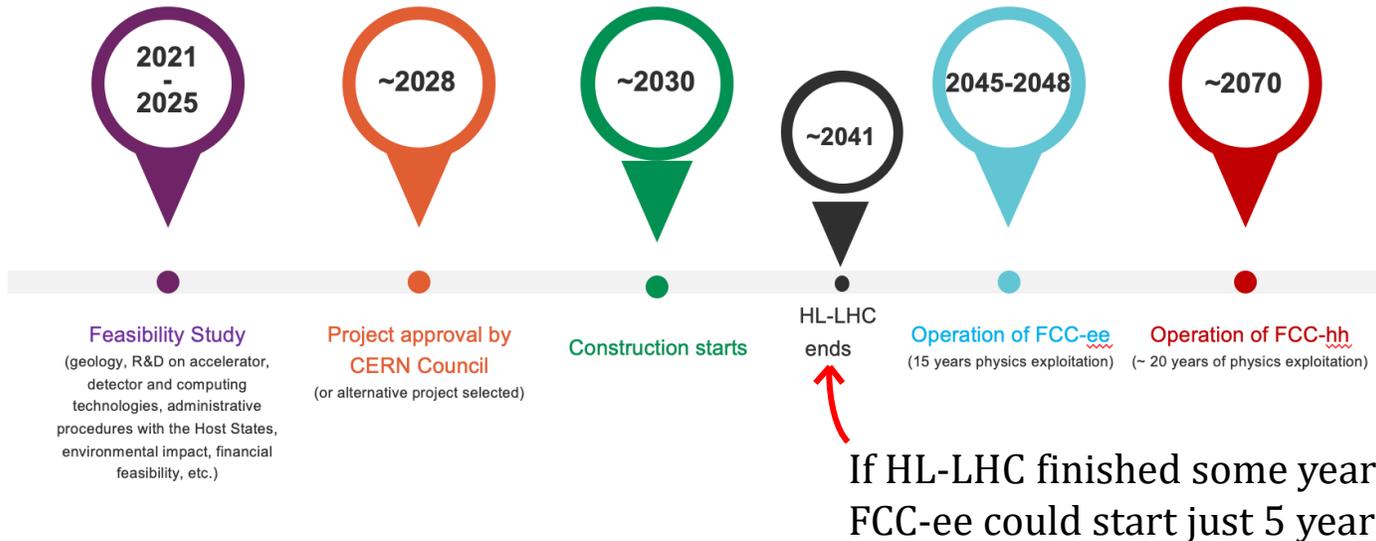
The FCC project

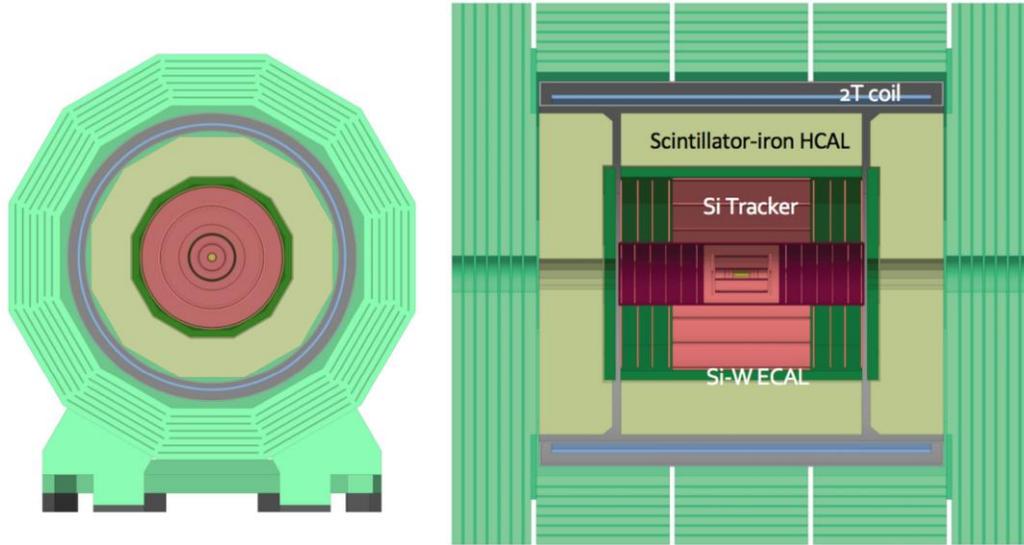2 main accelerator facilities in 100 Km tunnel have been studied:

- ee-collider (FCC-ee), as a potential first step

- pp-collider (FCC-hh), 100 TeV with 16T magnets

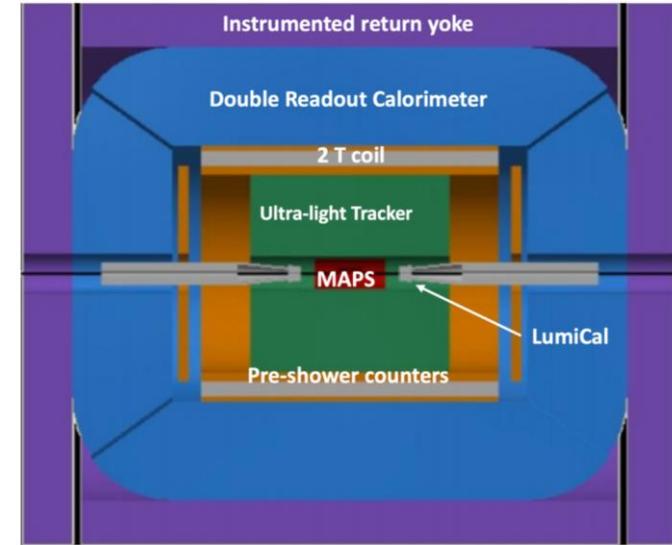with an additional option:

- ep-collider (FCC-eh)

2021 - 2025
Feasibility Study
(geology, R&D on accelerator, detector and computing technologies, administrative procedures with the Host States, environmental impact, financial feasibility, etc.)

~2028
Project approval by CERN Council
(or alternative project selected)

~2030
Construction starts

~2041
HL-LHC ends

2045-2048
Operation of FCC-ee
(15 years physics exploitation)

~2070
Operation of FCC-hh
(~ 20 years of physics exploitation)

If HL-LHC finished some years earlier FCC-ee could start just 5 years later

FCC – ee

CLIC-Like Detector (CLD)

- Silicon vertex detector
- Silicon tracker
- 3D-imaging highly granular calorimeter system
- Coil outside the calorimeter system

Innovative Detector for E⁺e⁻ Accelerators (IDEA)

- Silicon vertex detector
- Short-drift, **ultra-light** wire chamber
- Dual-readout calorimeter
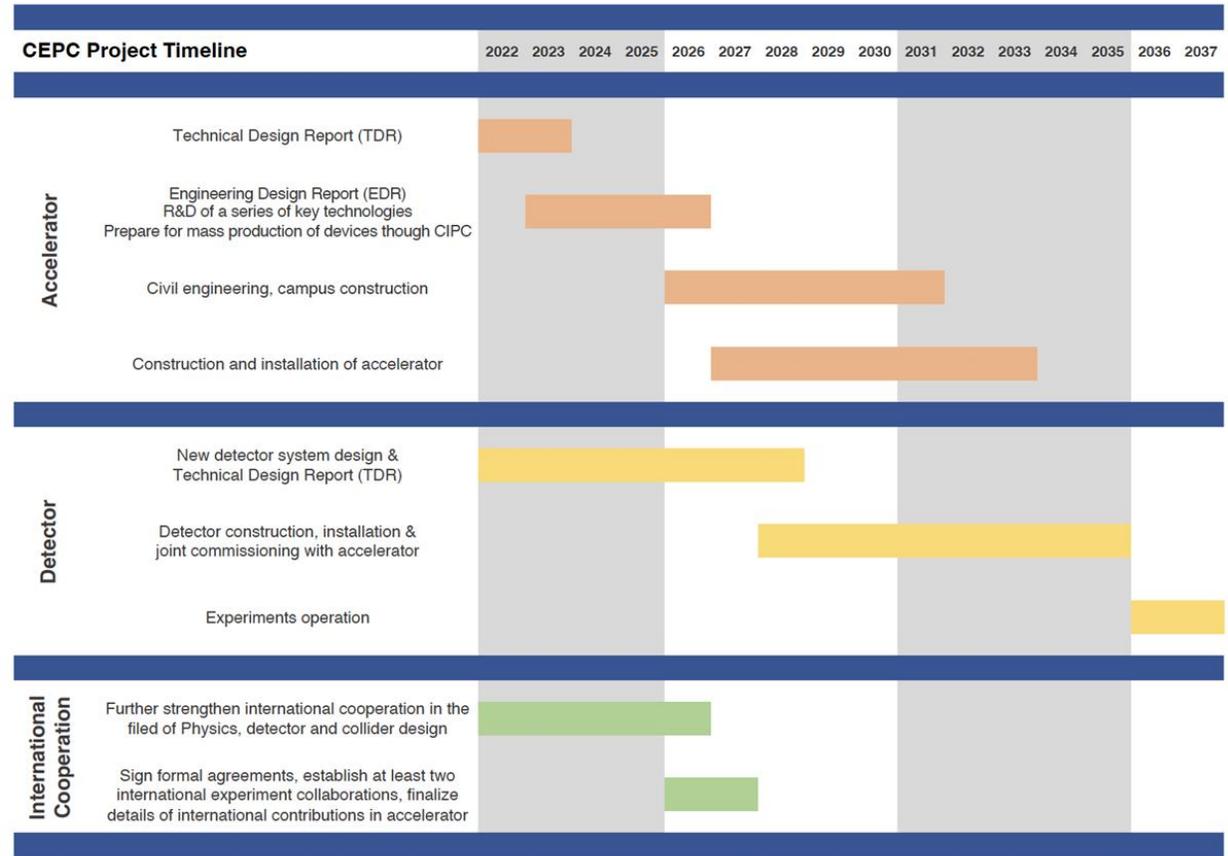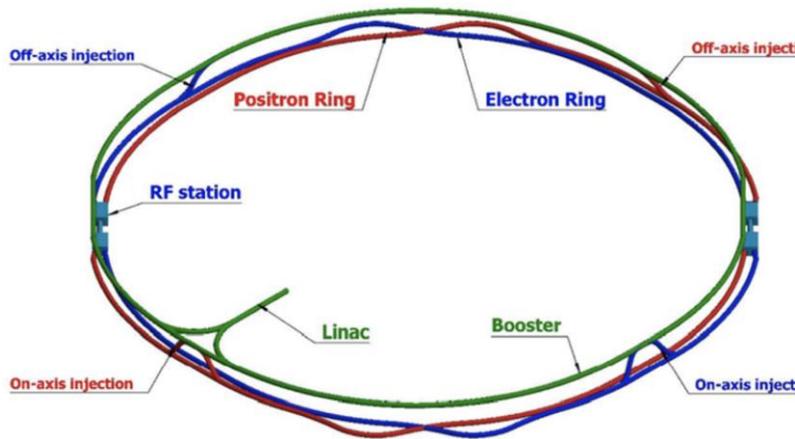- **Thin and light** solenoid coil **inside** calorimeter system

CEPC

Accelerator aimed to reach ~ 240 GeV as a first step and 50-100 TeV in the far future with a possible pp collider (SppC).
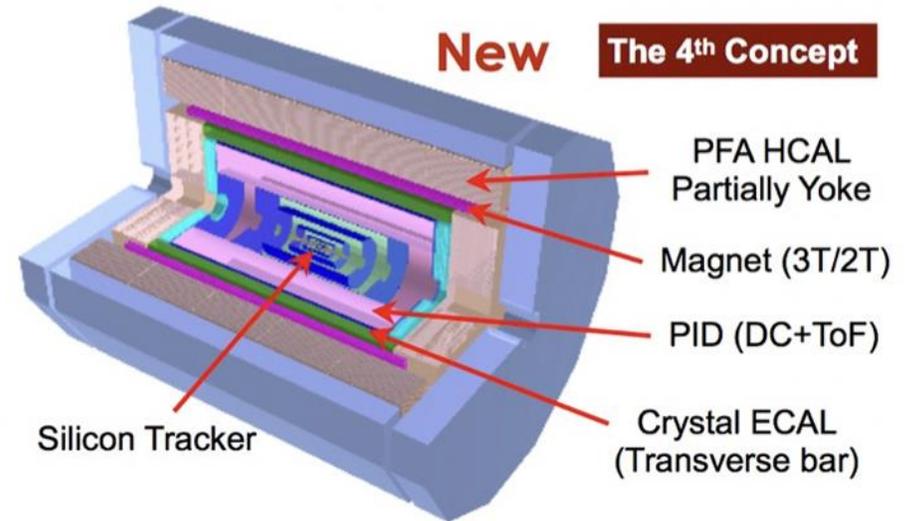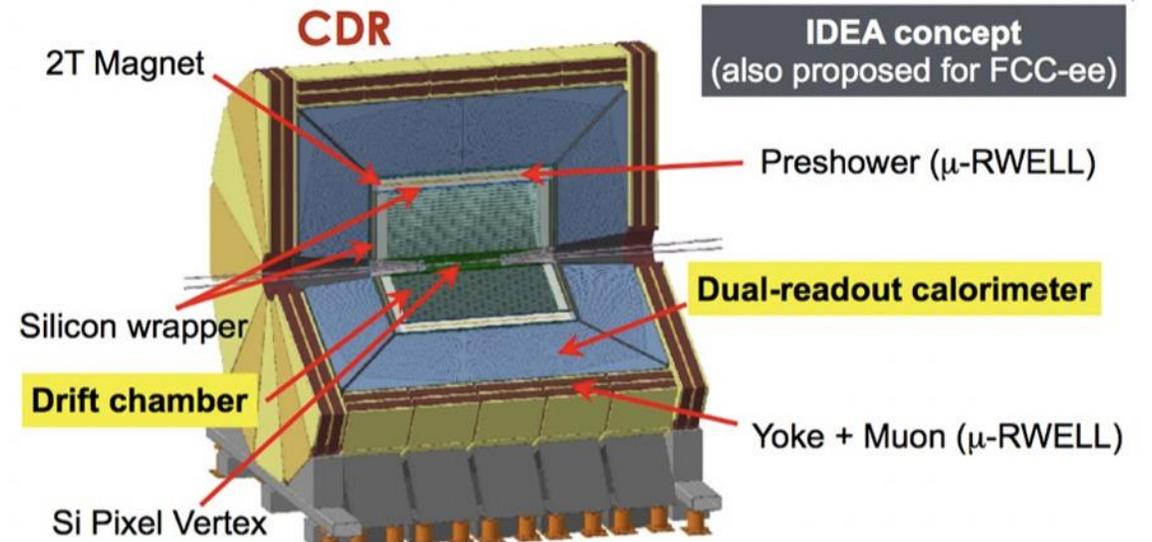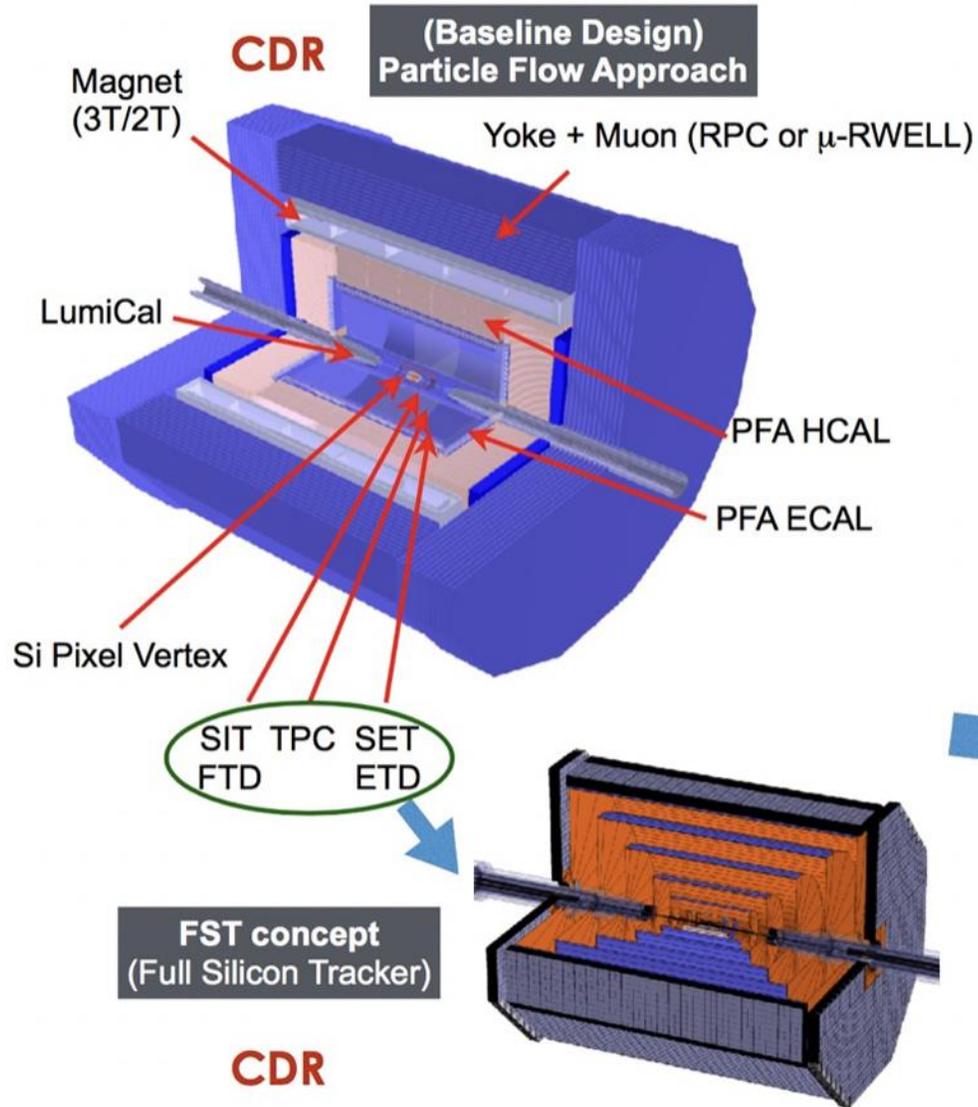

TDR (2023), EDR(2026), start of construction (2027-8)

- Circular collider
- 100 km circumference: optimum total cost, good also for SppC
- Shared tunnel: can accommodate CEPC booster and collider, SppC in the future
- Switchable operation: Higgs, W/Z, top
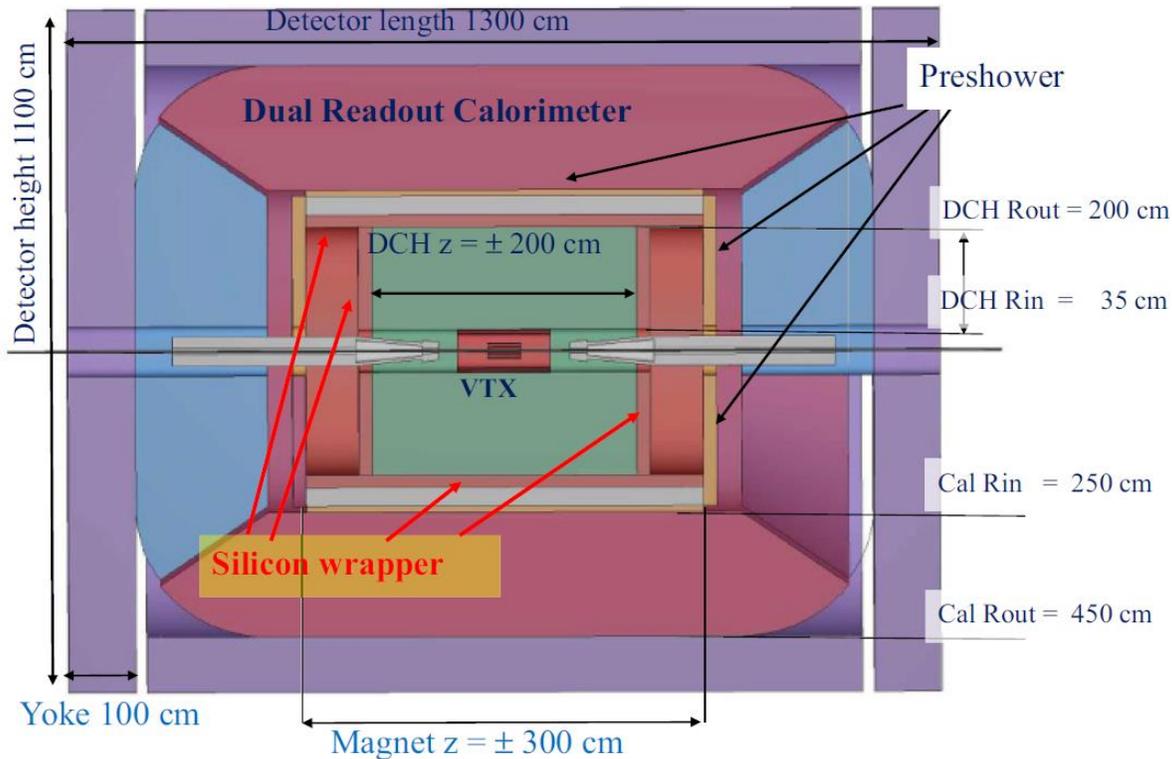
CEPC detector designs

From Jianbei Liu slides

IDEA detector layout

IDEA is a general-purpose detector designed for experiments at future e⁺e⁻ colliders, like FCC-ee and CEPC.

The **preshower** detector and the **muon system** are designed to be instrumented with **µRwell technology**.
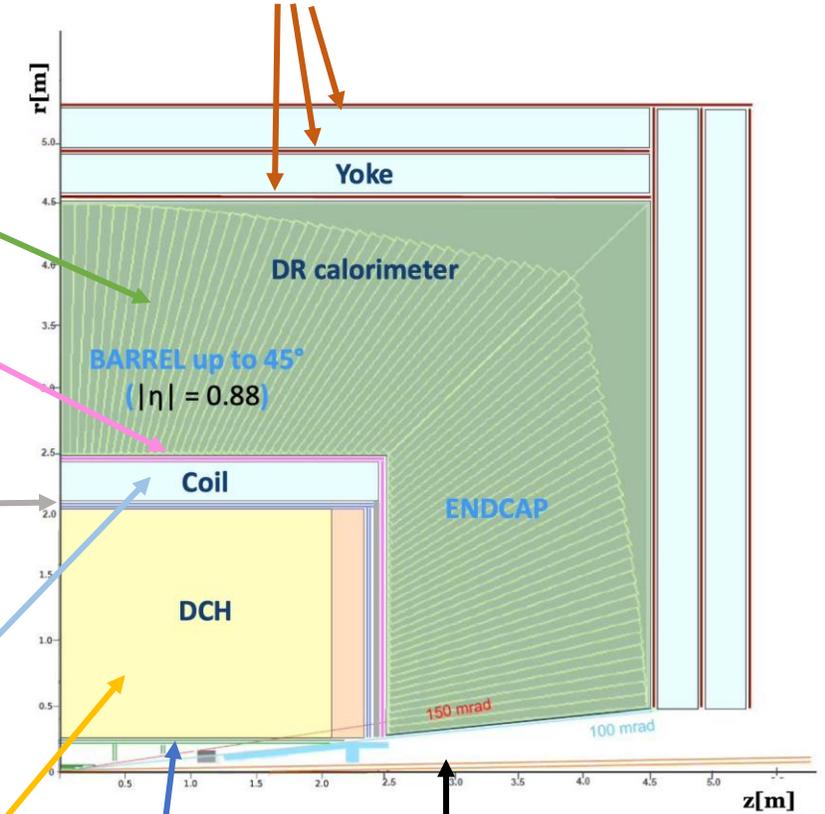
Muon System: 3 layers of µRwell

Dual-readout calorimeter: $2m$, $7\lambda_{int}$

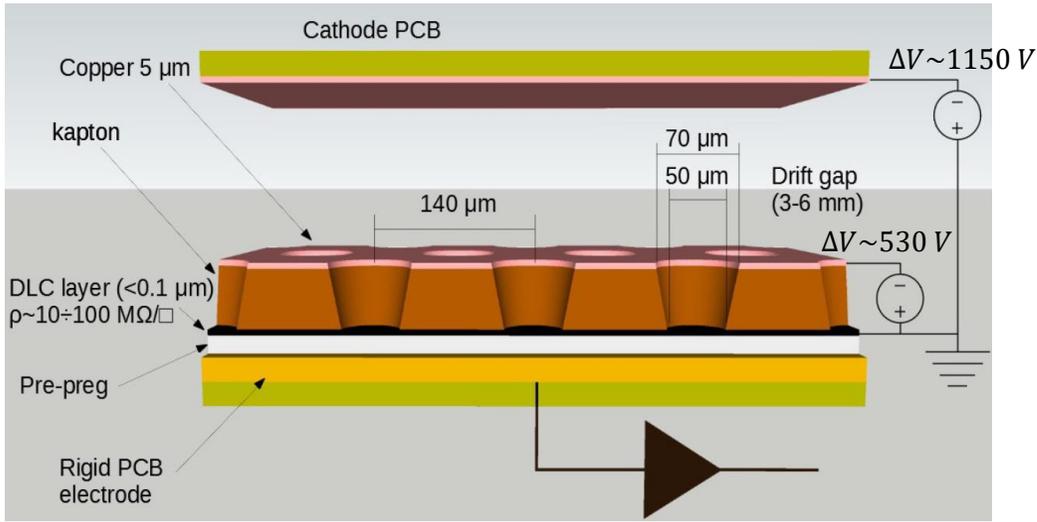**Preshower**: $\sim 1\ X_0$

Outer Silicon wrapper: Si strips

Superconducting solenoid coil: 2T, $R \sim 2{,}1 - 2{,}4\ m$, $0{,}74 X_0$, $0{,}16\lambda$ @ 90°

Drift Chamber: 112 layers, 4m long, $R = 35 - 200\ cm$, 1,6-5% X_0

VERTEX: 5 MAPS layers $R = 1{,}2 - 34\ cm$

Beam pipe: $R \sim 1{,}0\ cm$

Detector length 1300 cm

Dual Readout Calorimeter

DCH Rout = 200 cm

DCH z = ± 200 cm

DCH Rin = 35 cm

Preshower

VTX

Silicon wrapper

Cal Rin = 250 cm

Cal Rout = 450 cm

Detector height 1100 cm

Yoke 100 cm

Magnet z = ± 300 cm

r[m]

Yoke

DR calorimeter

BARREL up to 45° (|η| = 0.88)

Coil

DCH

ENDCAP

150 mrad

100 mrad
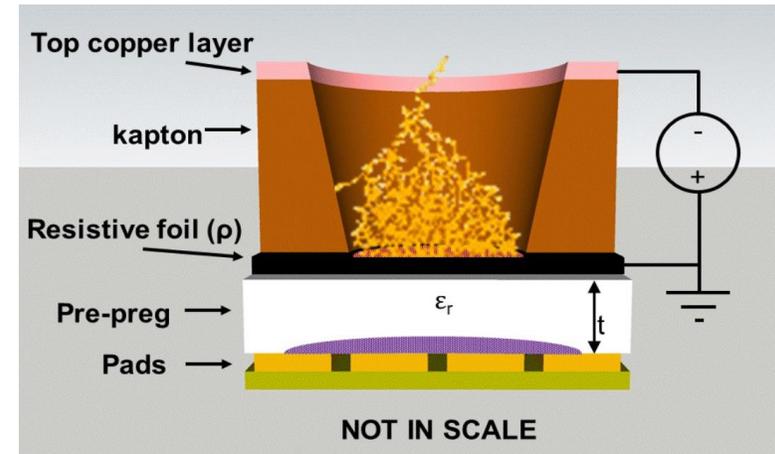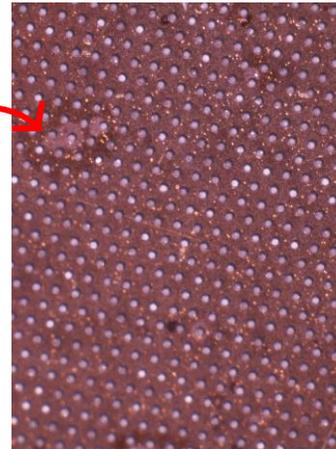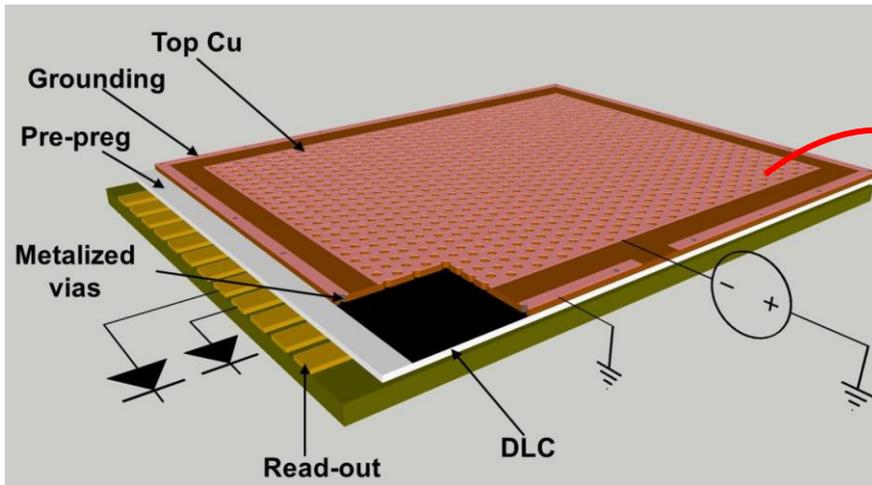
z[m]

μRwell technology

The *micro-Resistive well* is a resistive MPGD composed of two elements:

1. **Cathode**

2. μ-Rwell **PCB**
   - a **WELL** patterned **kapton foil** acting as amplification stage
   - a resistive Diamond-Like Carbon (**DLC**) layer, $\rho \sim 10 \div 100 \ M\Omega/\square$
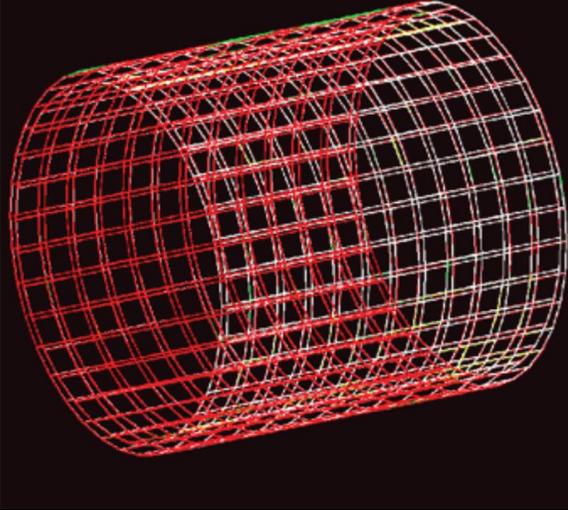   - a standard **readout PCB** with **pad** or **strip** segmentation

The **well** act as a multiplication channel for the ionization produced in the drift gas gap

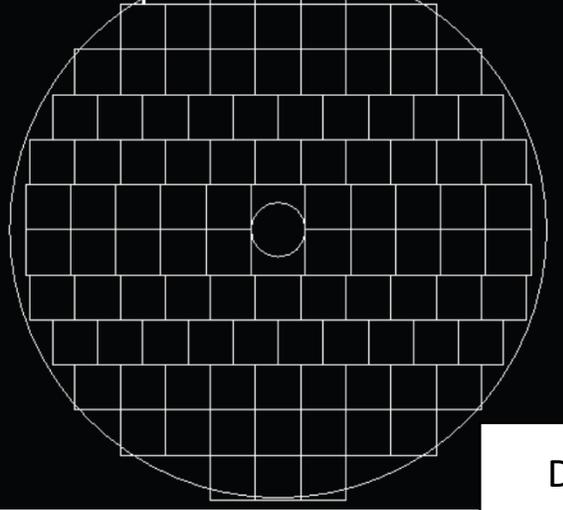The **resistive** stage ensures the spark amplitude quenching

G. Bencivenni et al., The micro-Resistive WELL detector: a compact spark-protected single amplification-stage MPGD, 2015 JINST 10 P02008

IDEA's preshower

Barrel Preshower

Endcap Preshower

Example of detector sector made of square μRwell tiles overlapped in 2 dimensions to minimise dead area as much as possible

Provides high resolution after the magnet to improve cluster reconstruction

Foreseen readout:
- Strip pitch: 0,4 mm
- Strip length: 50 cm
- FEE capacitance: 70 pF
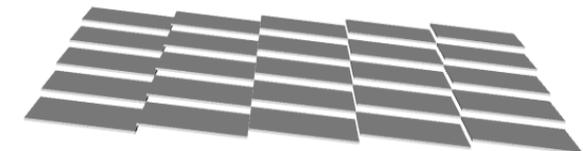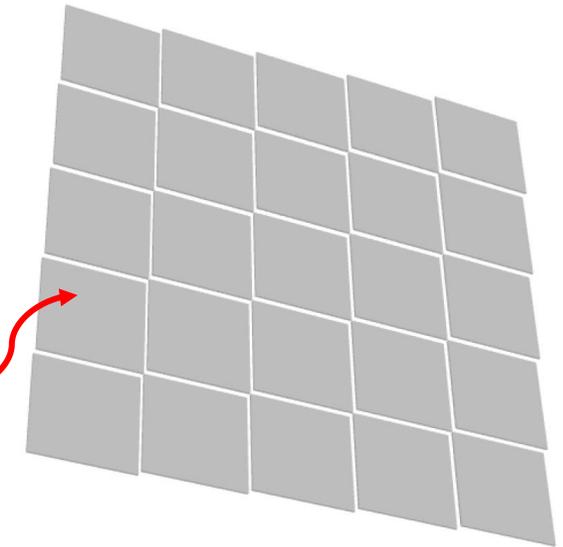- **Area : 130 m²**
- Channels: 1,3 M

Requirements:
- Efficiency > 98%
- Spatial resolution < 100 μm

Detector technology:
μRwell

50x50 cm² tiles with X-Y readout

IDEA's muon detector

Identifies muons and searches for LLPs

Foreseen readout:
- Strip pitch: 1,2 mm
- Strip length: 50 cm
- FEE capacitance: 270 pF
- **Area : 1530 m^2 [*]**
- Channels: ~5 M

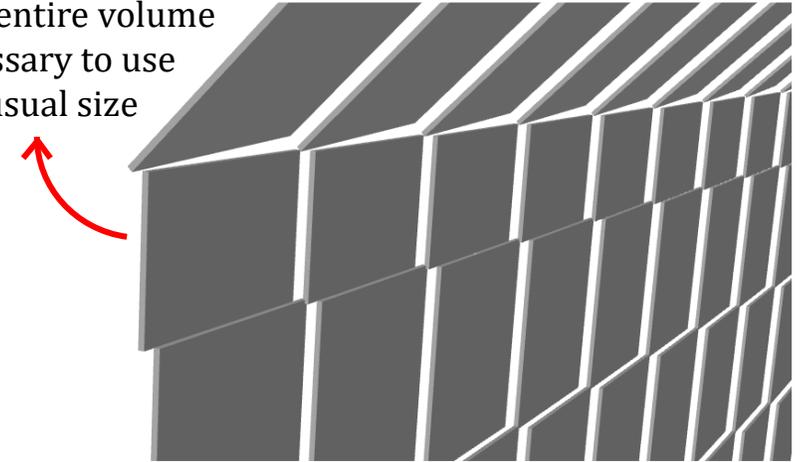Requirements:
- Efficiency > 98%
- Spatial resolution < 400 μm
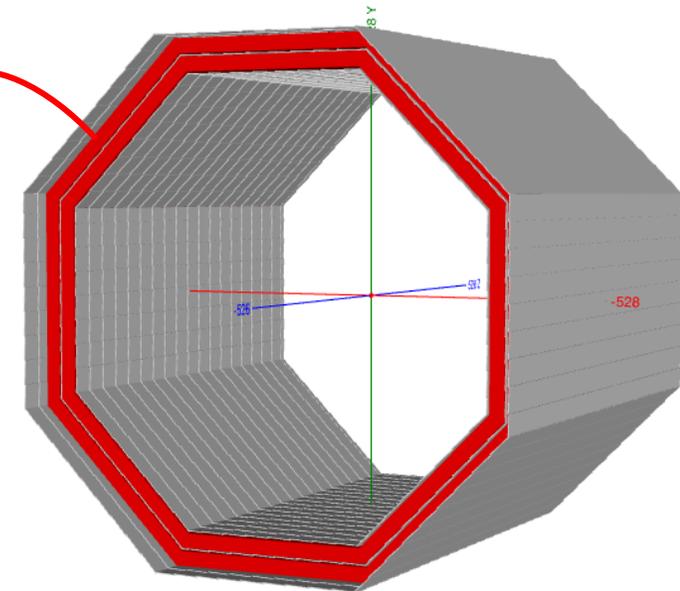
Detector technology:
μRwell

50x50 cm^2 tiles with X-Y readout

To cover the entire volume may be necessary to use blocks of unusual size

Iron yokes
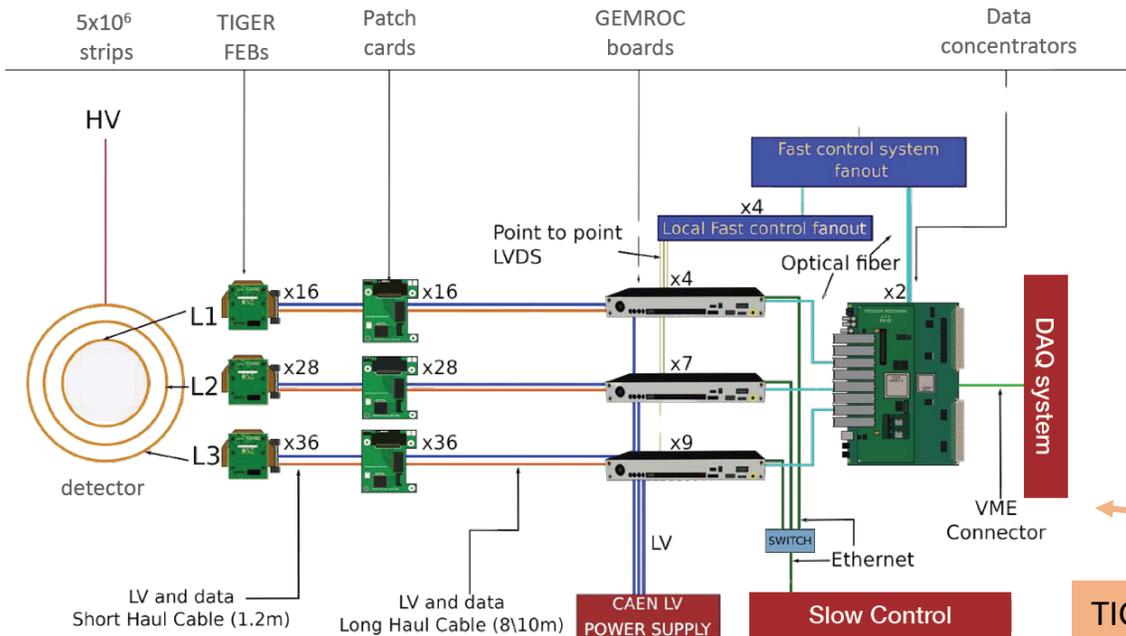
[*] Need for mass production ⇒ Technology Transfer to Industry

μRwell technology: readout with TIGER electronics

- Robust **DAQ with APV25**, as a first step

- Readout tested with TIGER ASIC, developed for BESIII CGEM-IT.
  - First working setup installed and **tested with 10x10 cm^2 μRwell** prototype
  - 64 channels
  - Noise level very low ($\sim 1\ fC$)

- Future: development of a **dedicated ASIC for μRwell**

Measured performance of the TIGER ASIC.

Parameters	Values
Input charge	5-55 fC
TDC resolution	30 ps RMS
Time-walk (5-55 fC range)	12 ns
Average gain	10.75 mV/fC
Nonlinearity (5-55 fC range)	0.5%
RMS gain dispersion	3.5%
Noise floor (ENC)	1500 e^-
Noise slope	10 e^-/pF
Maximum power consumption	12 mW/ch

TIGER/GEMROC readout scheme for CGEM

Test beam results : 1D μRwell
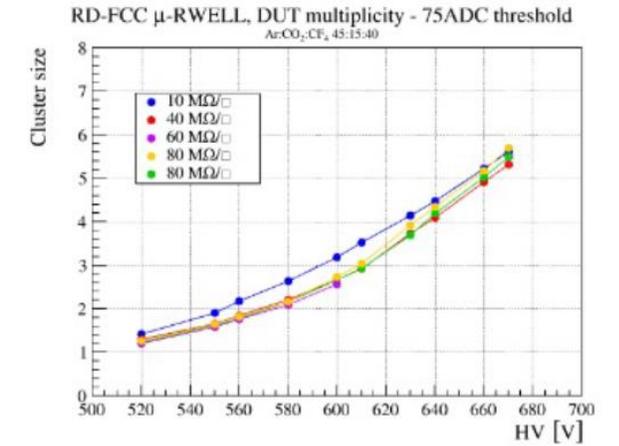
2021 - Resisitivity scan at fixed pitch

- Active area = 400x50 mm^2
- **Resistivity = 10-80 $M\Omega/\square$**
- Strip pitch = 0,4 mm
- Strip width = 0,15 mm
- Pitch/width ratio = 2,66

⟹ **Same** performance except for the 10 $M\Omega/\square$ prototype.
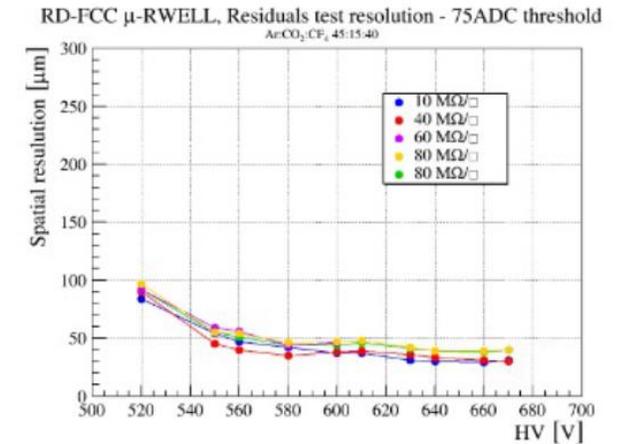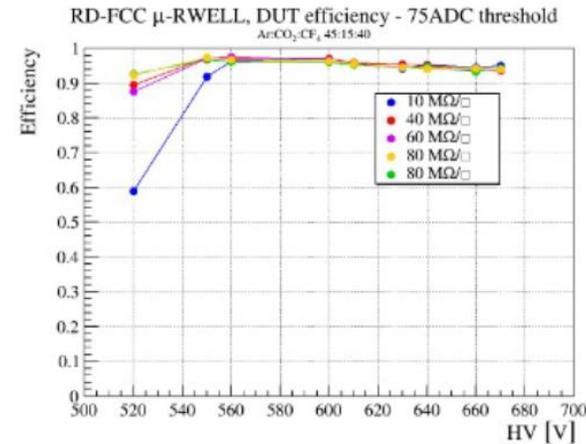**Efficiency knee** at **550 V**, $\sigma_x < 100\ \mu m$

(a) Cluster charge for different HV.
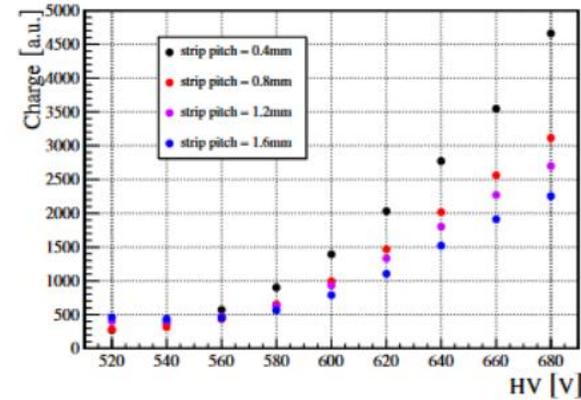
(b) Strip cluster size for different HV.

Test beam results : 1D μRwell
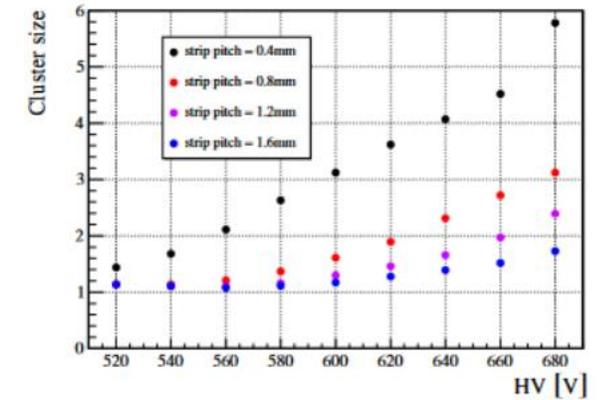
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$\Longrightarrow$ **Same** performance except for the 10 $M\Omega/\square$ prototype.
Efficiency knee at **550 V**, $\sigma_x < 100\ \mu m$

2022 - **Readout pitch** scan at **fixed resistivity**

- Active area = 400x50 mm^2
- Resistivity = 30 $M\Omega/\square$
- **Strip pitch = 0,4-1,6 mm**
- Strip width = 0,15 mm
- Pitch/width ratio = 2,66-10,66

$\Longrightarrow$ Larger the strip pitch, lower the charge signal requiring a higher gain to reach full efficiency.
Efficiency knee at **600 V**, $\sigma_x < 400\ \mu m$ **for 1,6 mm pitch**
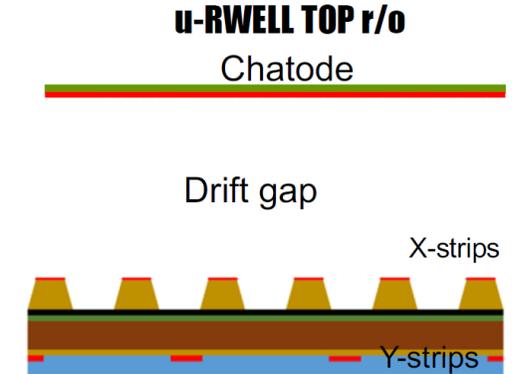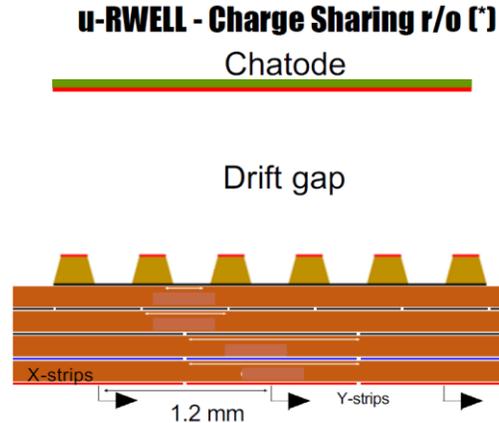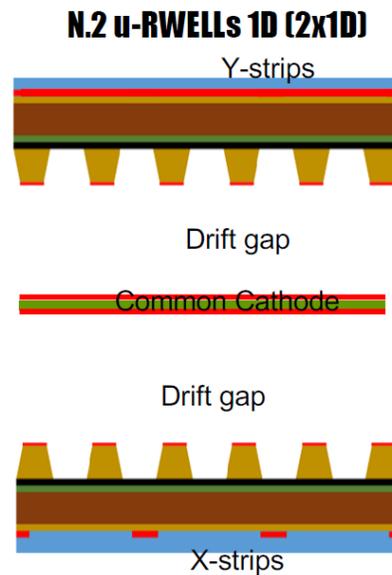

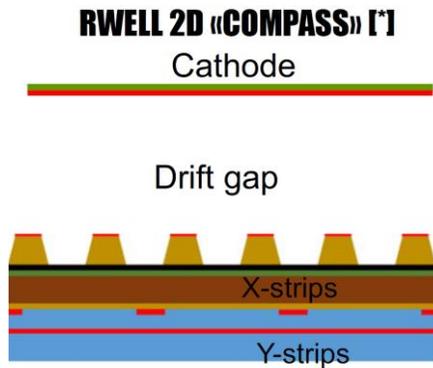(a) Cluster charge for different HV.

(b) Strip cluster size for different HV.

(c) Tracking efficiency for different HV.

(d) Residuals width for different HV.

μRwell technology: possible 2D layouts

RWELL 2D «COMPASS» [*]

Cathode

Drift gap

X-strips

Y-strips

- Good performance
- No easy optimization of the charge sharing on X-Y views
- Requires higher gas gain due to the coupling of the X and Y strips

(*) Y. Zhou et al. NIMA 927 (2019) 31

N.2 u-RWELLs 1D (2x1D)

Y-strips

Drift gap

Common Cathode

Drift gap

X-strips

- This option allows to work at lower gas gain wrt the «COMPASS» readout
- No volume optimization

u-RWELL - Charge Sharing r/o [*]

Chatode

Drift gap

X-strips   Y-strips

1.2 mm

Charge transfer and charge sharing using capacitive coupling between a stack of layers of pads and the readout board.
- Reduces the FEE channels.
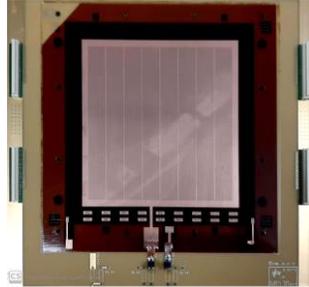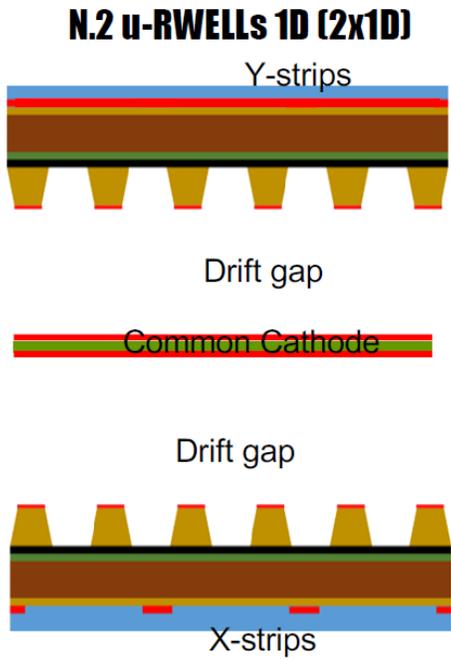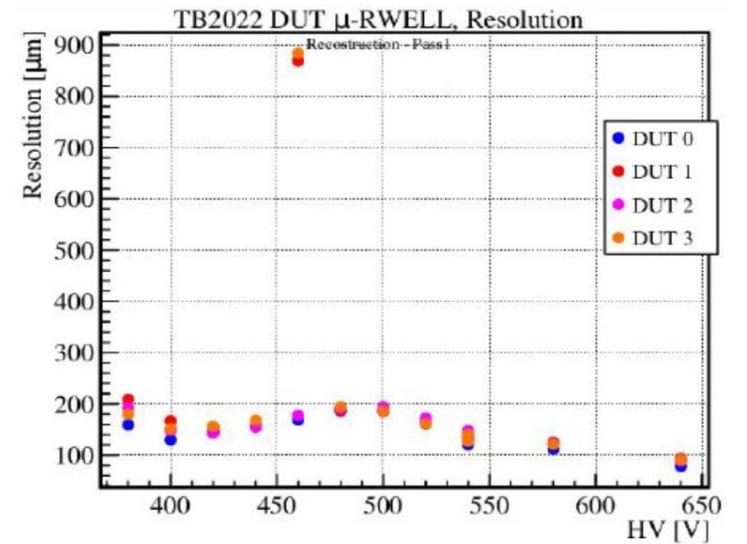- Total charge divided between X and Y readout (similar to the «COMPASS» readout).

(*) K. Gnanvo et al. NIMA 1047 (2023) 167782

u-RWELL TOP r/o

Chatode

Drift gap

X-strips

Y-strips

- The TOP layout allows to work at lower gas gain wrt the «COMPASS» readout
- X-Y readout are decoupled
- X coordinate on the TOP of the amplification stage introduces same dead zone in the active area
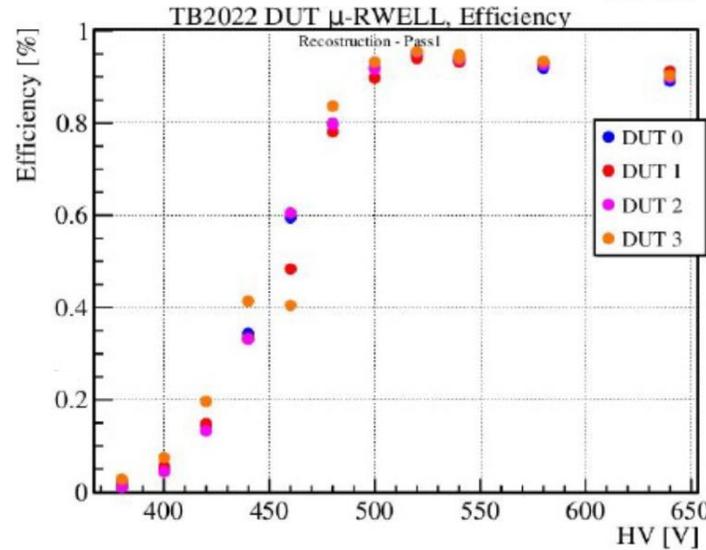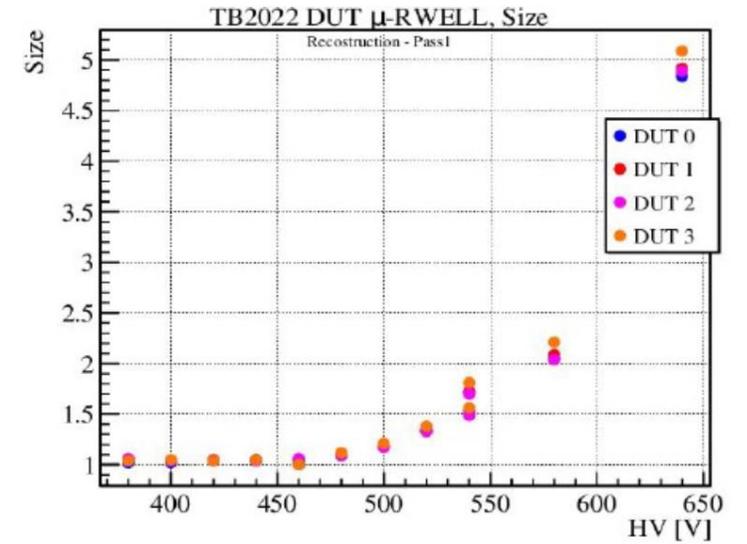
Test beam results : 2x1D µRwell

N.2 u-RWELLs 1D (2x1D)

Active area = 100x100 mm^2
Resistivity = 50 $M\Omega/\square$
Strip pitch = 0,76 mm
Strip width = 0,3 mm
Pitch/width ratio = 2,53

Efficiency knee at **500 V**,
$\sigma_x < 200\ \mu m$

Test beam results : 2D µRwell
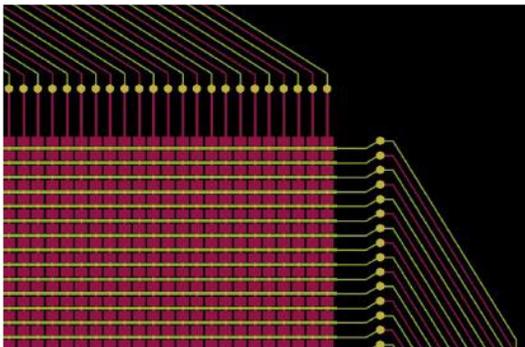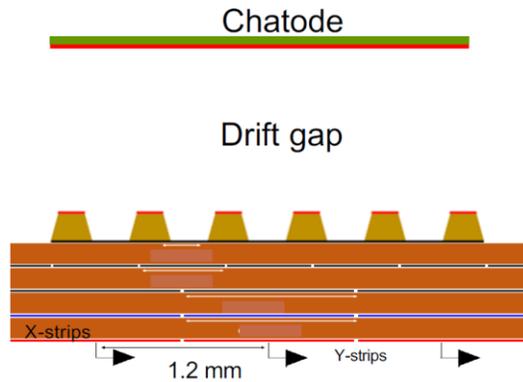
u-RWELL - Charge Sharing r/o (*)

Chatode

Drift gap

X-strips ◄ 1.2 mm ► Y-strips ►

Active area = 100x100 mm²
Resistivity = 50 $M\Omega/\square$
Strip pitch = 1,2 mm
Strip width = 1,1 mm

u-RWELL TOP r/o

Chatode

Drift gap

X-strips

Y-strips

Active area = 100x100 mm²
Resistivity = 50 $M\Omega/\square$
Strip pitch = 0,8 mm
Strip width = 0,7 mm
Dead zone (TOP) ~ 15%

Preliminary results

TB2023 µ-RWELL, Charge

TB2023 µ-RWELL, Size

TB2023 µ-RWELL, Efficiency

TB2023 µ-RWELL, Resolution

Test beam results : 2D μRwell

Charge Sharing readout

- **Total charge** is **divided between X and Y views** (by construction)
- **Cluster size** increases up to **4 strips** (proof that the charge sharing mechanism works)

- **Efficiency knee** at **600 V**
- **High efficiency plateau** (~**95%**)
- **Spatial resolution** improves at higher gain reaching **150 μm** with a strip pitch of 1,2 mm

Preliminary results

TOP readout

- The **total charge** is **not divided between X and Y strips** (by construction)
- **Cluster size** does **not change on X axis** (TOP layer), while **improves on the Y axis**, due to the DLC spread

- **Efficiency knee** at **500 V** (like the 1D prototype)
- **Low efficiency plateau** (~**70%**) due to the dead area introduced by TOP readout
- **Digital spatial resolution** on the X axis (strip size 1,5 mm), improving on the Y axis

Technology transfer with ELTOS*

PCB production @ ELTOS

µRwell TT — INFN LNF / AIDA innova

µRwell_PCB:
- Amplification stage
- Resistive stage
- Readout plane

DLC foil production @ CERN / INFN

Detector Manufacturing — CERN

DLC Magnetron Sputtering machine co-funded by INFN-CSN1

* <u>Eltos | Circuiti Stampati Professionali</u>

Summary: 2023 Status

- **Finalization of the TB 2022 analysis** with µRwell prototypes with **1D strip readout**
  - 100x100 mm^2 active area & 0,76 mm strip pitch
  - 50x400 mm^2 active area & 0,4-1,6 mm strip pitch
  - ▶ Allowed to select the best parameters (strip pitch and resistivity) to get high efficiency and resolution with minimum gain

- **Production of µRwell** with **2D strip readout** (100x100 mm^2 active area):
  - TOP readout – 0,76 mm strip pitch
  - Charge sharing readout – 1,2 mm strip pitch

- **Beam Test** (NA-H8C, 14-28 June 2023) of the 2D layouts, performed with APV25.

- **Finalization of TB 2023 analysis.** Comparison of the 2D performance: 2D layout (CS & TOP) vs 2x1D layout.
  - ▶ The 2x1D layout has more reliable performance with high gain at low voltage and a constant resolution around 200 µm, with the volume drawback. CS and TOP layouts require still some optimization to improve space resolution and/or efficiency.

2024 Program

Study
- Study **gas gain optimization** with **different geometries of the amplification stage** (pitch well, external/internal well diameters) with 100x100 mm^2 prototypes. **[*]**
- With a reduction of the well pitch from 140 μm to 90 μm, a possible **increase of the gas gain of about 2** is foreseen.

Development
- Development of a new ASIC based on the knowledge acquired with TIGER.

Production
- **n°2 500x500 mm^2 prototypes** (second half of 2024): the choice of 2D layout will be based on the results obtained in the previous test.

Test
- Equipe a μRwell chamber with TIGER.
- Test of a large 2D technology prototype at CERN.
- Test at LNF with X-ray and cosmics (with tracking system).
- Test of the mRwell processes at ELTOS/CERN and DLC machine (CERN).
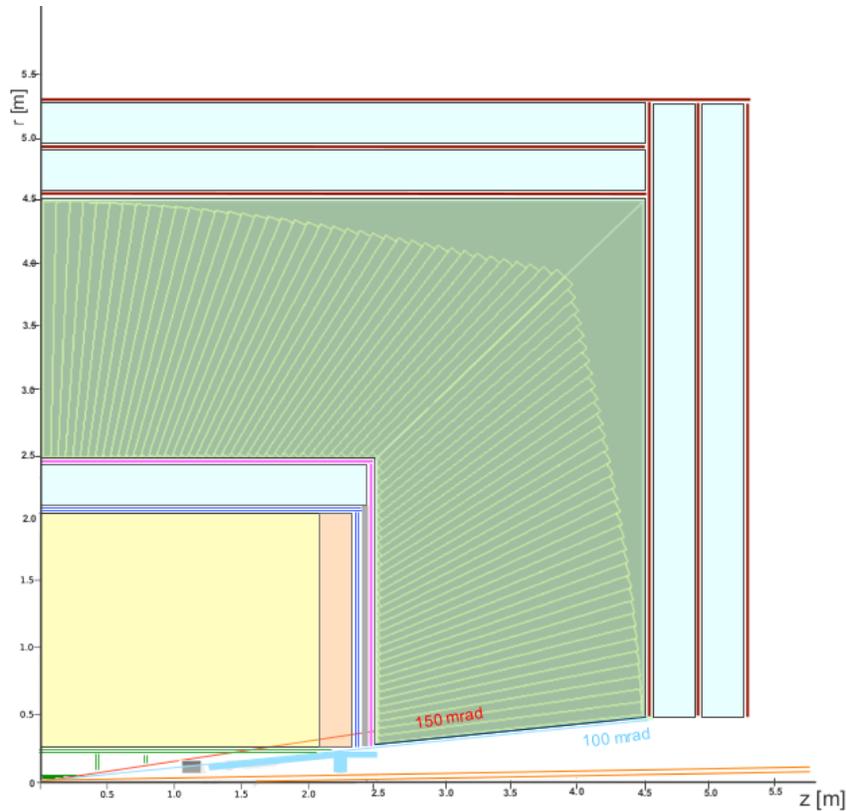
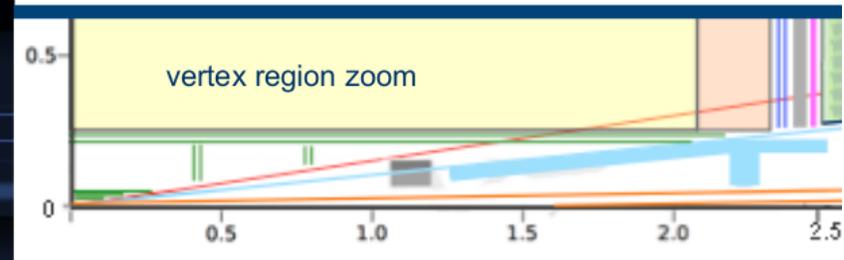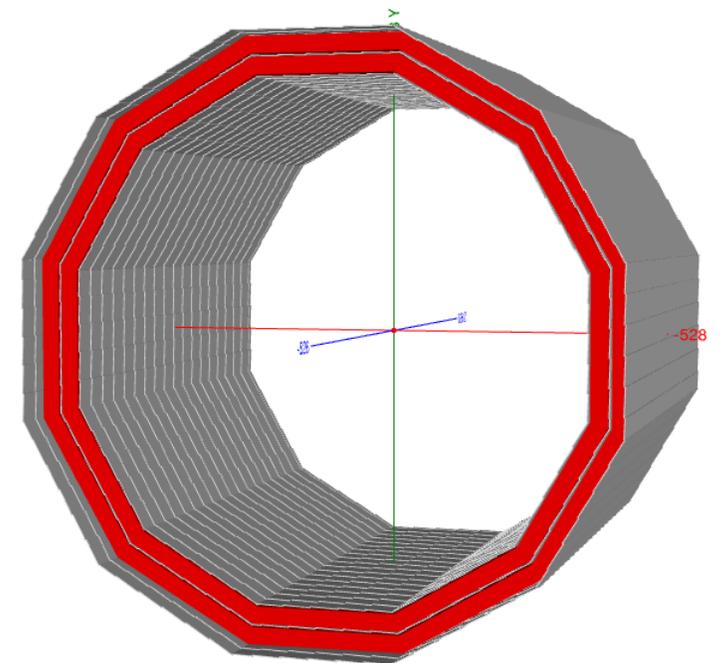[*] These studies have been performed with GEM detector but never with mRwell.

The End

Backup slides

IDEA geometry

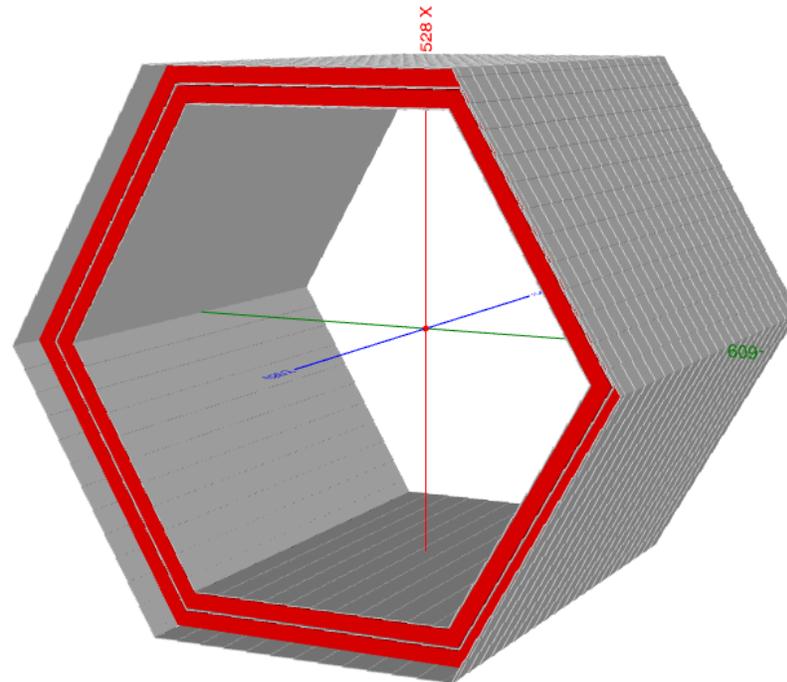**LEGENDA**

- drift chamber
- drift chamber service area
- magnet and iron return yoke
- calorimeter
- Si pixels — 20μm×20μm (inner barrel layers), 50μm×1mm (outer barrel layers), 50μm×50μm (forward disks)
- Si strips double stereo layer 50μm×10cm
- μRwell double layer 0.4mm×50cm
- μRwell double layer 1.5mm×50cm
- absorber (lead)
- luminometer
- steel simulating compensating and shielding solenoids
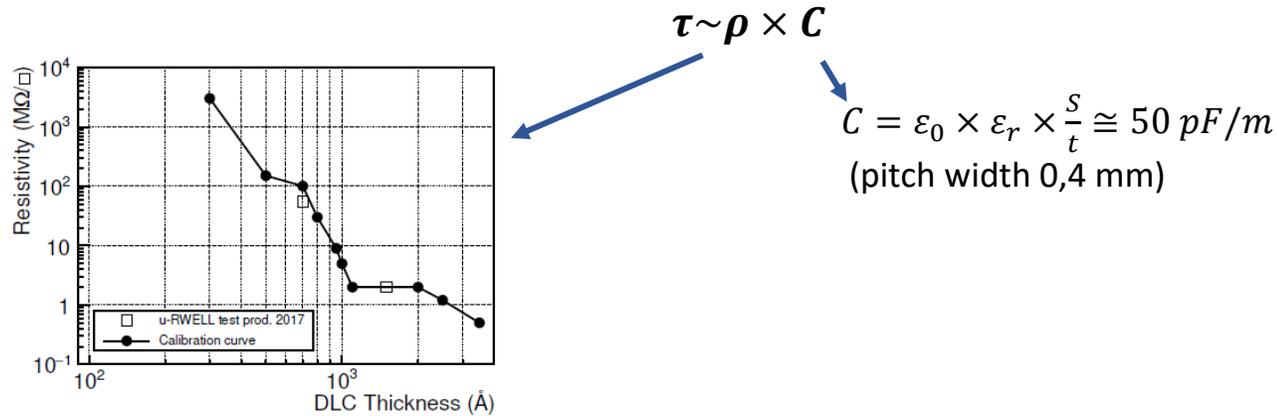- vacuum tube

vertex region zoom

IDEA's Muon System

Starting from a simple cylindrical shape for both Muon System and Preshower, it is possible to simulate different layouts for the detectors.
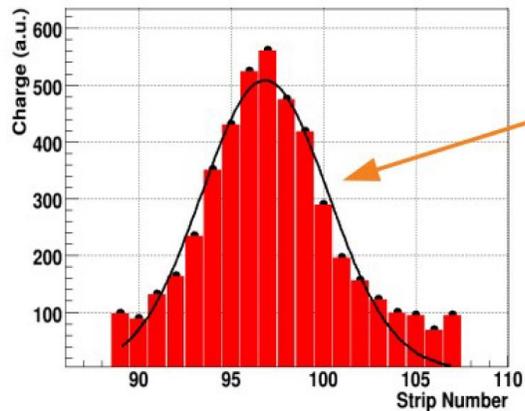
Charge collection and multiplication

- The "WELL" acts as a multiplication channel for the ionization produced in the gas of the drift gap

- The **charge induced** on the resistive layer is **spread with a time constant**

$$\tau \sim \rho \times C$$

$$C = \varepsilon_0 \times \varepsilon_r \times \frac{S}{t} \cong 50 \; pF/m$$

(pitch width 0,4 mm)

Charge distribution for different ρ

Resistivity

Charge collected by the APV25 on the strip readout (resistivity ~ $10 \; M\Omega/\square$)

APV25 and 400 μm strip pitch: capacity = 15 pF

G.Bencivenni et al., "Performance of μ-RWELL detector vs resistivity of the resistive stage", NIM A 886 (2018) 36

High rate layout

- The resistive stage ensures the spark amplitude quenching.

- Drawback: capability to stand high particle fluxes reduced, but largely recovered with appropriate grounding schemes of the resistive layer
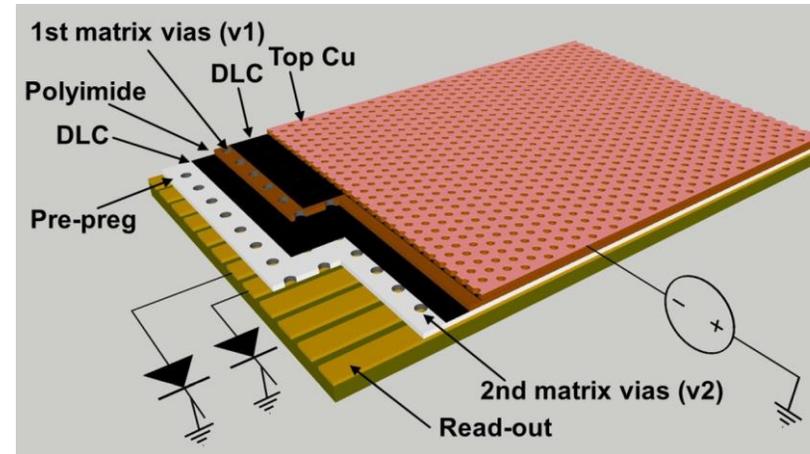
Single-Resistive layout (SRL)	**Double-Resistive (DR) layout**	**Single-Grid (SG) layout**

- Single DLC layer
- Large d (~ active area size)
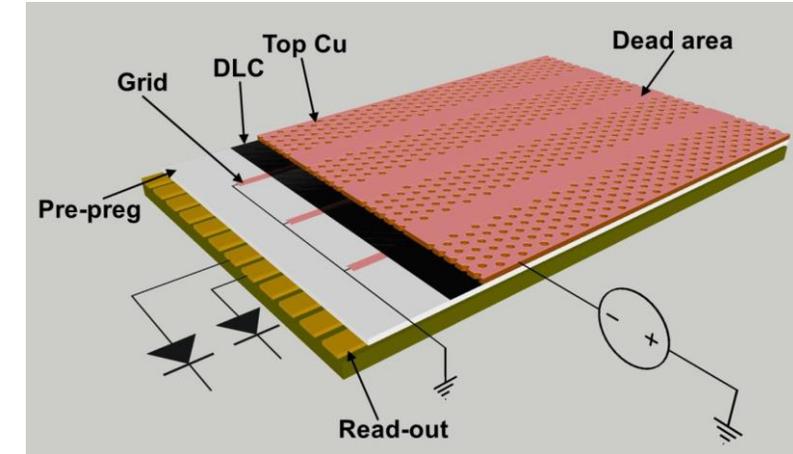- **Low rate** purposes (up to 100 kHz/cm^2)
- **Easy** for industry

- Stack of DLC foils interconnected by a matrix of conductive vias
- d ~ 1 cm
- **High rate** purposes (> 10 MHz/cm^2)
- **Complex manufacturing**
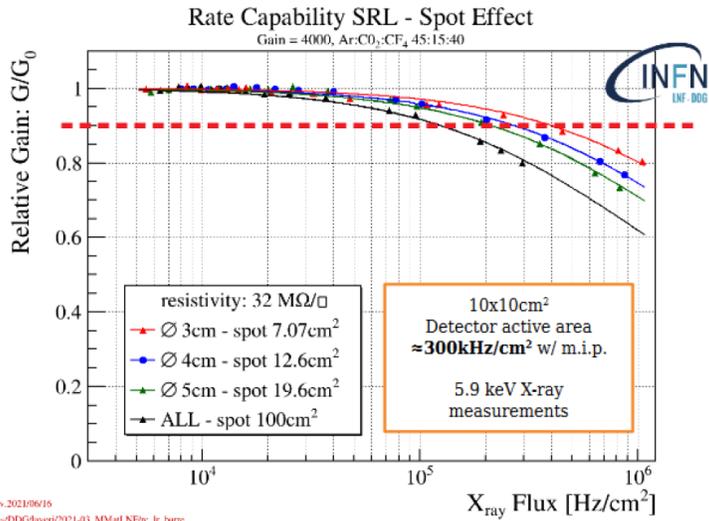
- DLC grounded by coated Cu strips below
- d ~ 1 cm
- **High rate** purposes (> 10 MHz/cm^2)
- **Complex Cu + DLC sputtering**
- **Difficult alignment** of the grounding lines with the dead areas on top of the amplification stage (especially for large size detectors)
- **95%** geometrical **acceptance**

d = average distance to the ground

High rate layout

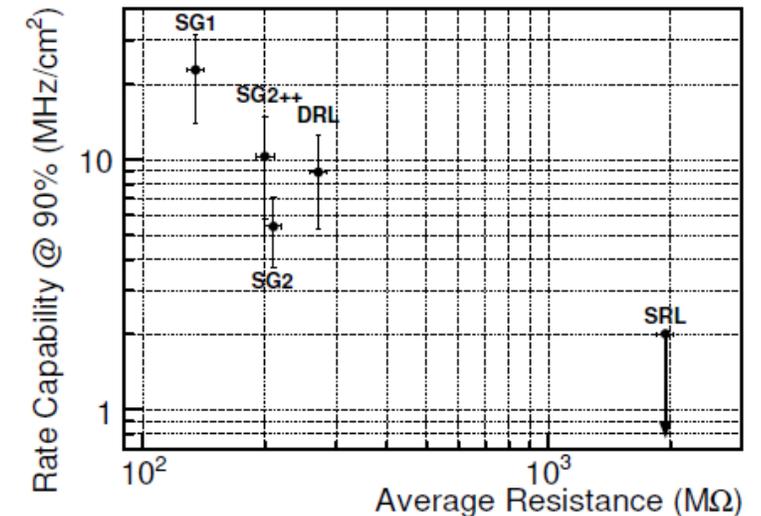$$[*] \quad \frac{G}{G_0} = \frac{-1 \pm \sqrt{1 + 4p_0\varphi}}{2p_0\varphi}$$

$$\Omega(r) = \frac{p_0(r)}{\alpha e N_0 G \pi r^2}$$
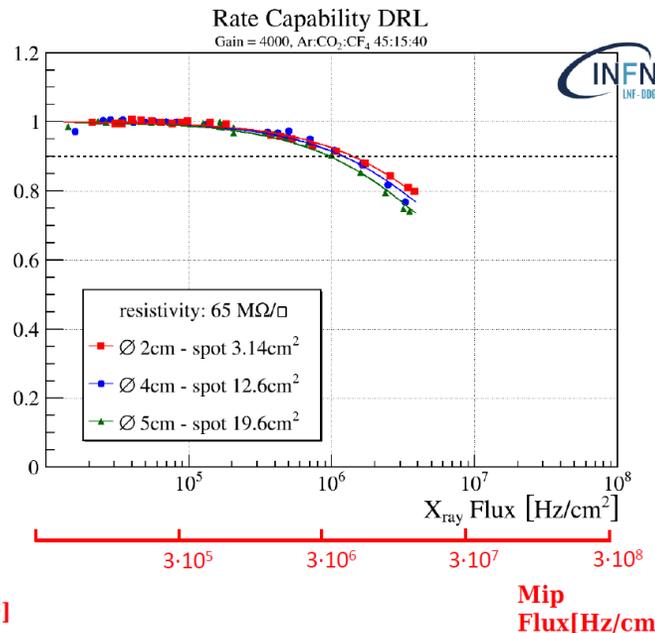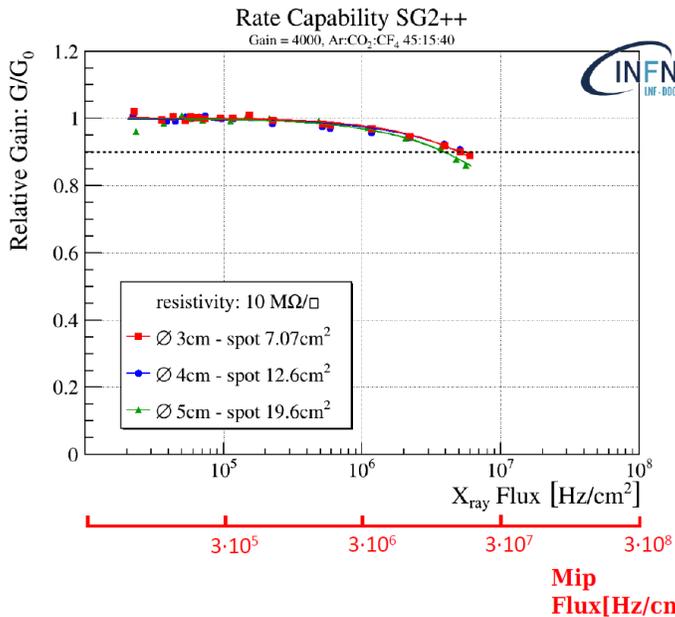
$$= \rho_S \frac{d - \dfrac{r}{2}}{\pi r}$$

Naif model for the *average resistance* Ω between the charge collection point and the perimetrical grounding line

$\boldsymbol{\alpha}$ from the fit to the gain vs. applied ΔV
$\boldsymbol{N_0}$ from GARFIELD++ simulation
$\boldsymbol{r}$ radius of the X-rays spot
$\boldsymbol{d}$ average distance to the ground

Capacitive Sharing readout: Principle & Motivation (K.GNAVO)

- Vertical stack of pad layers: charge transfer via capacitive coupling

- Pads have dedicated position from one layer to the layer underneath

- Doubling in size at each layer

- Transverse sharing of the charges between neighbouring pads of layer ($i+1$) from vertical charge transfer from layer (i)

- The scheme preserves spatial information *i.e.* the spatial resolution obtained with the largest readout strips or pads.
  $\implies$ Goal: 50 μm for 1 mm strip r/o
  150 μm for 1 cm^2 pad r/o

- Proof of concept established with 800 μm X-Y strips

AIM:

- Develop high performance and low channel count readout structures for MPGDs

- Reduce the number of readout electronic channels for large area MPGDs

- Low-cost technology for large area and standard PCB fabrication techniques
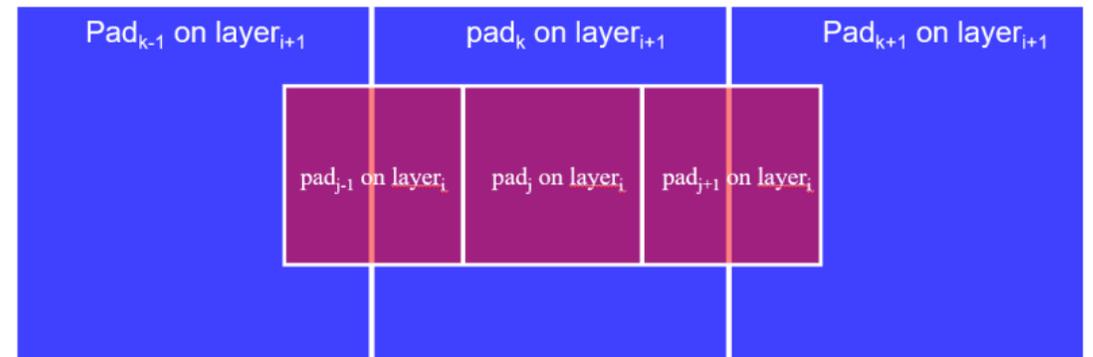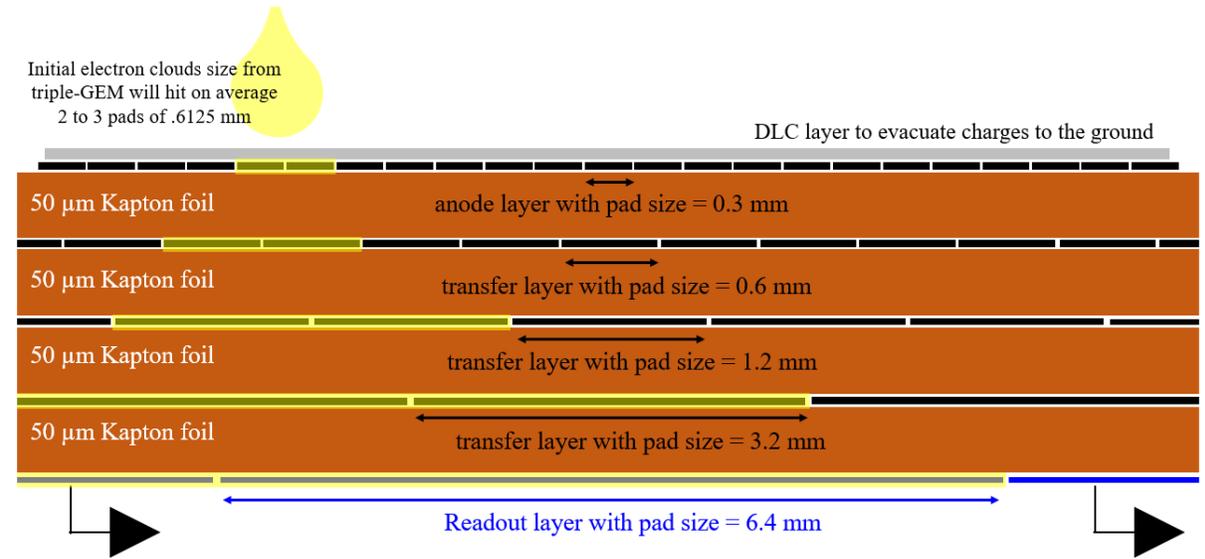
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