Updates on the Sampa project and an overview on the ALICE3 TOF system

FAPESP collaboration meeting
15/10/2024

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Summary:

Introduction

- The new version of the software: wiki and configuration management

New hardware

- The new hybrids
- The replicator board

ALICE 3

- The TOF
- CMOS results
- Next beam test

- **New configuration files input to migrate easier between experiments**
- **We are building a wiki (under construction):**

Home

geovanegrossi edited this page 3 weeks ago · 13 revisions

Welcome to the SampaSRS wiki! (under construction 🛠️)

The SampaSRS project

Acquisition

Processing data

The SAMPA ASIC

The SAMPA chip is an ASIC (Application Specific Integrated Circuit) developed at the Integrated Systems Laboratory (LSI) of the USP Polytechnic School (POLI) to serve the TPC and the Muon Chambers (MCH) of the ALICE experiment, operating at CERN.

SAMPA/FPGA configuration commands

List of commands

The list of commands available until now can be found below. This commands can be added to a *config.txt* file. Several commands require arguments to work.

- `start/stop` (start or stop the data transmission by SAMPA)
- `reset_fec` (reset the Front-End Card)
- `reset_sampas` (default reset for the chips - clear all configs and set the same initial timestamp)
- `reset_sampasHigh` (reset with different logic level - used just for tests)
- `trigger_1hz` (1 Hz internal trigger)
- `trigger_2.5khz` (2.5 kHz internal trigger)

Data decoding for later reconstruction:

Understanding the data structure

The data decoded is stored in a ROOT TTree file. Inside the directory `root_examples` you will find ways to access the data. Using it you can build your own algorithms to work with data.

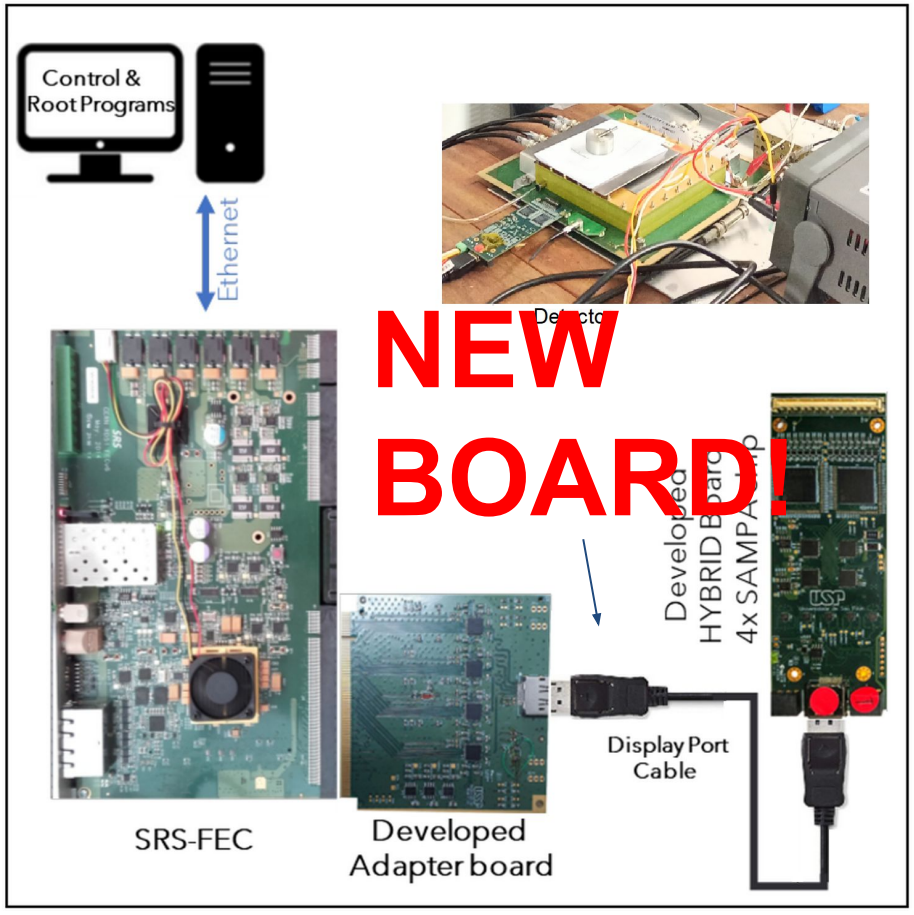
```
TTreeReader reader("waveform", &file);

TTreeReaderArray<short> sampa(reader, "sampa"); //vector with the SAMPA ID
TTreeReaderArray<short> channel(reader, "channel"); //vector with the channel ID
TTreeReaderValue<std::vector<std::vector<short>>> words(reader, "words"); // vector of vectors (with word i
TTreeReaderArray<double> x(reader, "x"); //vector with the geometry position of the channel

 int event_id = 0;
 while (reader.Next())  //read all events in file
 {
  auto& event_words = *words;
  for (size_t i = 0; i < event_words.size(); ++i)  //this loop over the active channels
  {
   gl_chn = 32*sampa[i]+channel[i];
   for (size_t j = 2; j < event_words[i].size(); ++j) //this loop over the waveform of a active channel
    {
    event_words[i][j];
    }
   }
 }
```

https://github.com/SampaSRS/SampaSRS

The complete setup

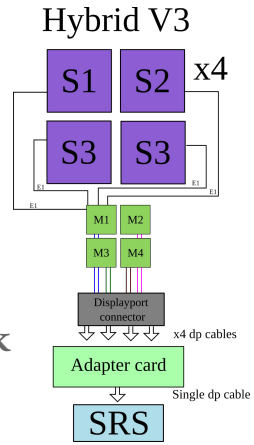


Hybrid v3 board overview:

Each hybrid provides 128 channels

Number of active links can be changed using just one multiplexer

Reduced bandwidth but possibility to work with multiple hybrids



Adapter board overview:

Each SAMPA chip is connected to one high speed serializer

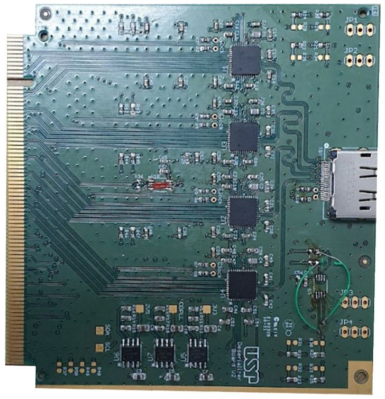
A single Display-Port cable is used to connect the hybrid and the adapter board

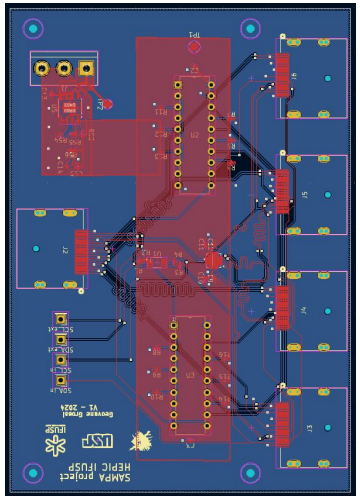
The adapter board has four deserializers and a PCIx16 standard to connect a Front-End Card (FEC).

FEC:

Ethernet communication limit to 1Gbit/s

Replicator V1:



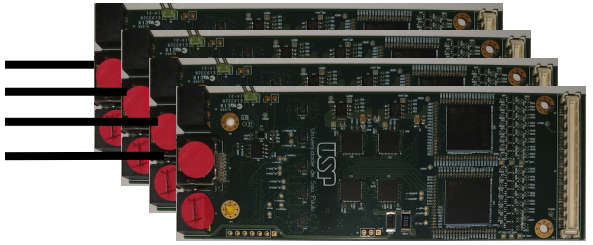


Routing all signals

Replicate clocks, RESET, I2C signals

The wires are crossed inside the displayport cable.

Integrate all the components into a single board - Reading up to 512 channels with each application.

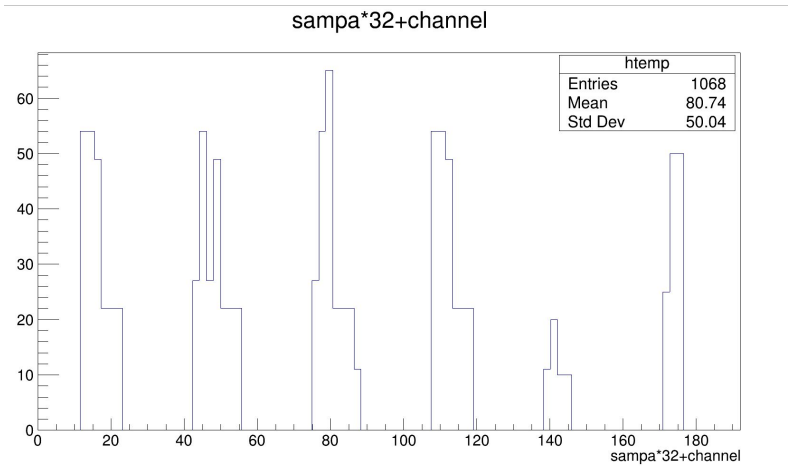


Wrong routing of the first differential pair

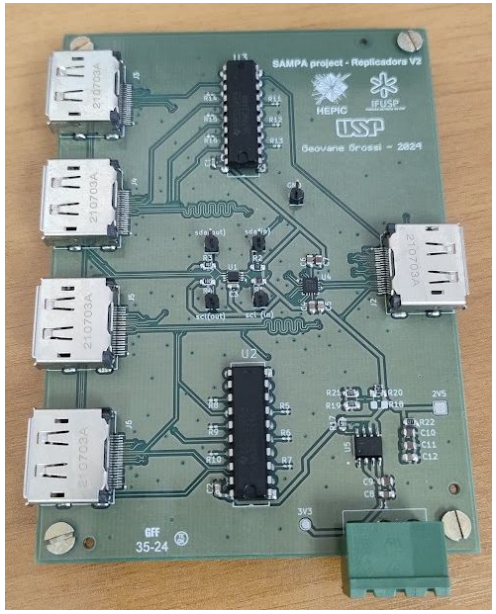
However, the replicator board works!

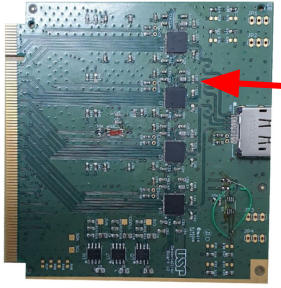
DisplayPort Standard Cable

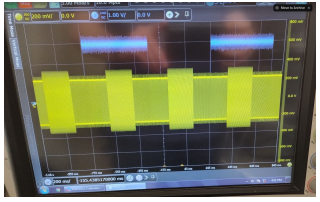
Source Side Plug			Cable Wiring	Sink Side Plug		
At SOURCE Signal Type		Pin#		Pin#	At SINK Signal Type	
Out	ML_Lane 0(p)	1		1	ML_Lane 3 (n)	In
GND	GND	2		2	GND	GND
Out	ML_Lane 0 (n)	3		3	ML_Lane 3 (p)	In
Out	ML_Lane 1 (p)	4		4	ML_Lane 2 (n)	In
GND	GND	5		5	GND	GND
Out	ML_Lane 1 (n)	6		6	ML_Lane 2 (p)	In
Out	ML_Lane 2 (p)	7		7	ML_Lane 1 (n)	In
GND	GND	8		8	GND	GND
Out	ML_Lane 2 (n)	9		9	ML_Lane 1 (p)	In
Out	ML_Lane 3 (p)	10		10	ML_Lane 0 (n)	In
GND	GND	11		11	GND	GND
Out	ML_Lane 3 (n)	12		12	ML_Lane 0 (p)	In
CONFIG	CONFIG1	13		13	CONFIG1	CONFIG
CONFIG	CONFIG2	14		14	CONFIG2	CONFIG
I/O	AUX_CH (p)	15		15	AUX_CH (p)	I/O
GND	GND	16		16	GND	GND
I/O	AUX_CH (n)	17		17	AUX_CH (n)	I/O
In	Hot Plug Detect	18		18	Hot Plug Detect	Out
	Return DP_PWR	19		19	Return DP_PWR	
	DP_PWR	20		20	DP_PWR	

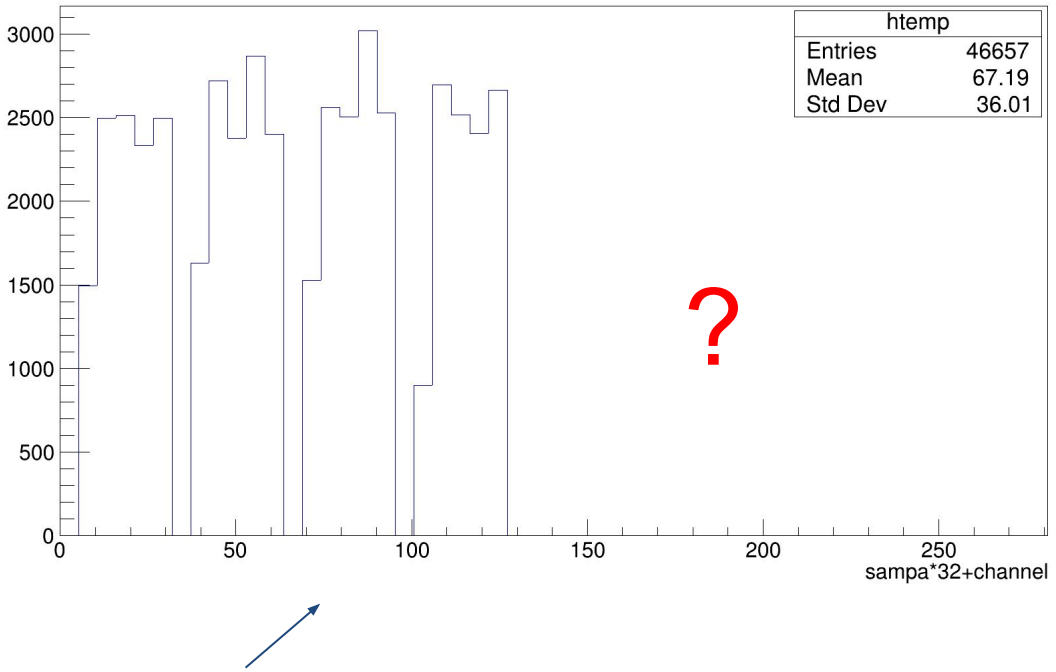


Replicator V2:





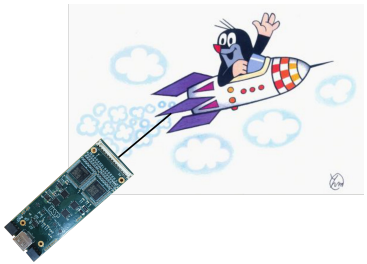




- The routing is correct
- I2C works properly but the board is unstable (demux clock issue?)
- We are planning the next step (go for a V3 - but we need this hardware working to continue to improve the software and start measurements

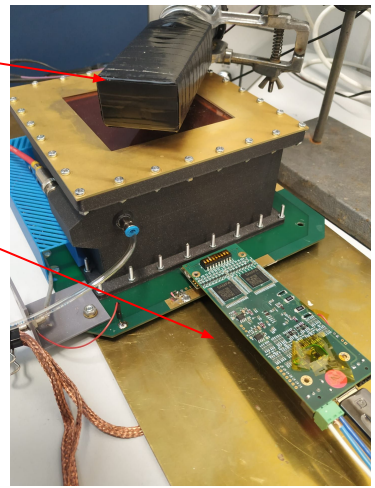
The SAMPA in the Czech Technical University in Prague - Work developed by Hugo N. Luz

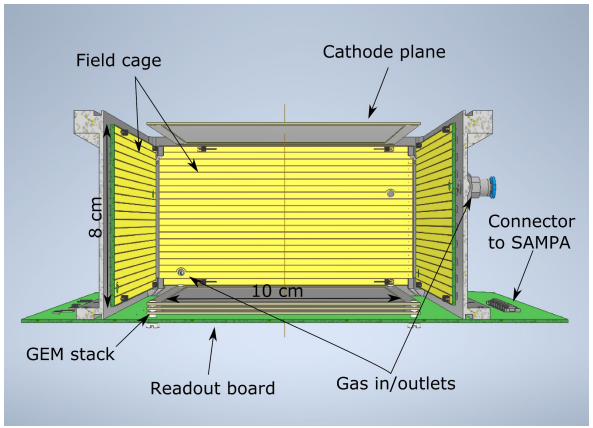
IEAP CTU in Prague



Scintillator+PMTs

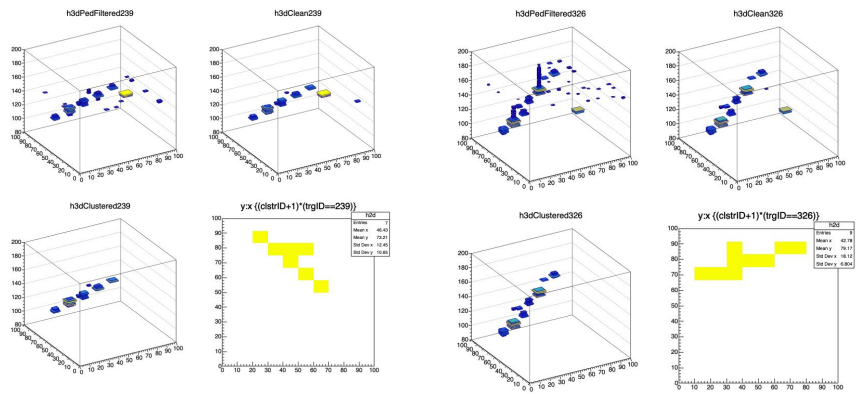
SAMPA hybrid



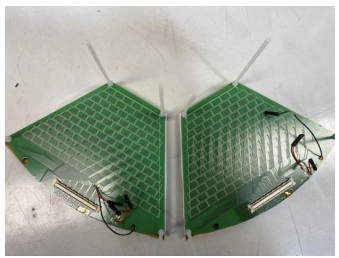


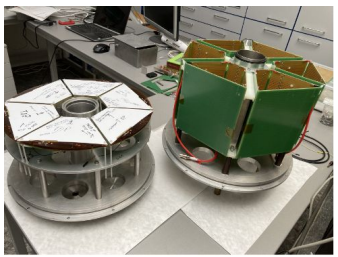
First TPC tracks ever with a small TPC
Achieved in Prague during my period there in 2021

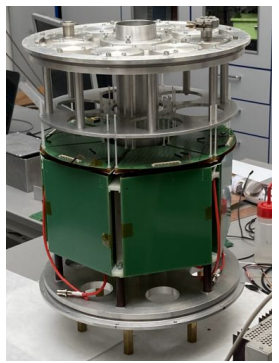
Matěj Gajdoš is working on track reconstruction usi NN - Poster presentation MPGD2024 - Hefei



Towards a spectrometer with 6 TPC







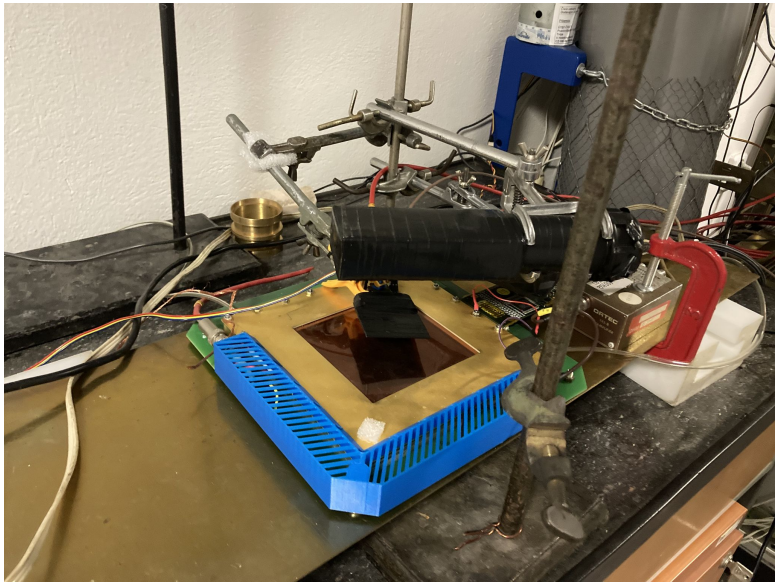
6 SAMPA hybrids will be mounted
(24 chips, 768 channels)

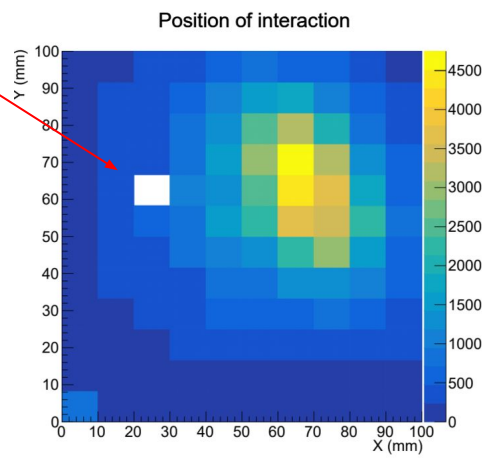
The SAMPA in the Czech Technical University in Prague - Work developed by Hugo N. Luz

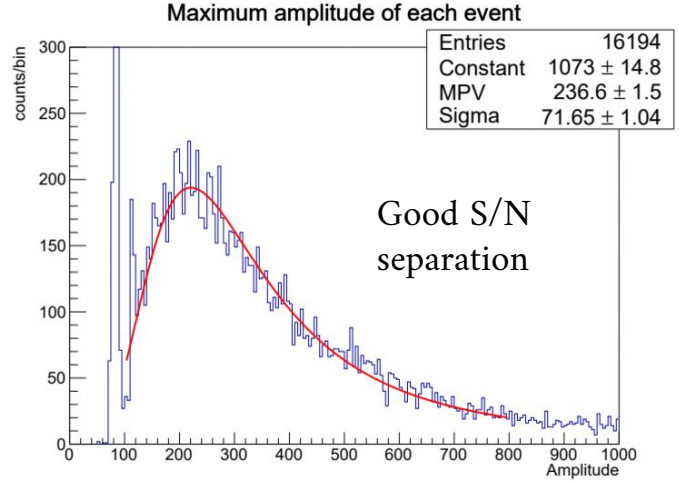
IEAP CTU in Prague

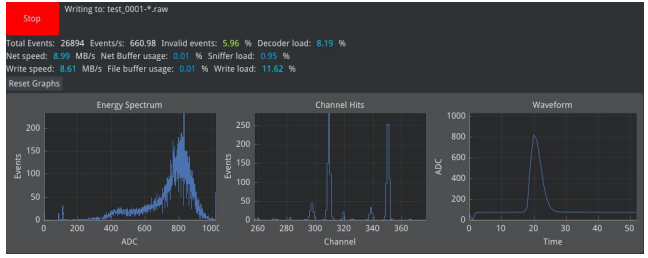
Most recent tests:

- 7 consecutive days under cosmics with completely stable operation in triple GEM detector (without field cage). 2 evts/min
- Problematic channel under investigation
- Event reconstruction on-going.









SampaSRS installed in the central computing facility and working

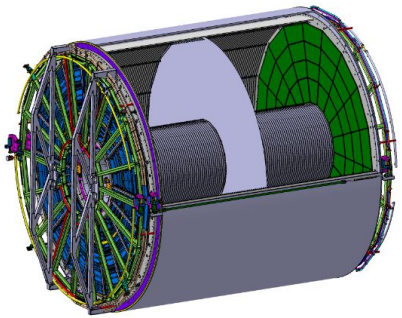
ALICE upgrades

Run 1 2009 - 2013 → **Run 2** 2015 - 2018 → **Run 3** 2022 - 2025 → **Run 4** 2029 - 2032 → **Run 5** 2035 - 2038 → **Run 6** 2040 - 2041

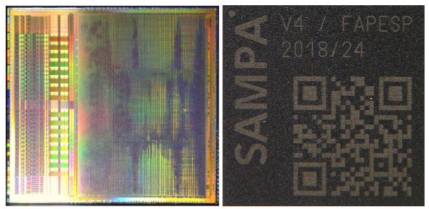
Run 1: pp, pPb, Pb-Pb
Run 2: pp, pPb, Xe-Xe, Pb-Pb

Run 3: pp, pO, OO, pPb, Pb-Pb
Highest energy proton-proton collisions at 13.6 TeV

Several upgrades:



- Multi-wires to GEMs
- SAMPA for the TP and MCH - continuous readout



3kHz limit for Pb-Pb (active ion gating grid) to 50 kHz with GEMs

- New ITS (7 layers - 10m² surface area - CMOS technology)
- New Muon Forward Tracker (MFT) - CMOS technology
- Upgrades on the readout, trigger and beam pipe and others

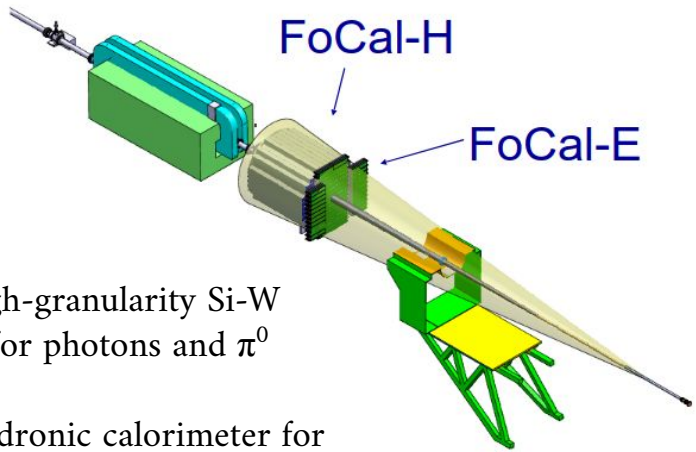
ALICE upgrades

Run 1 2009 - 2013 → **Run 2** 2015 - 2018 → **Run 3** 2022 - 2025 → **Run 4** 2029 - 2032 → **Run 5** 2035 - 2038 → **Run 6** 2040 - 2041

Run 4: pp, pPb, Pb-Pb

Forward Calorimeter

$3.2 < \eta < 5.8$

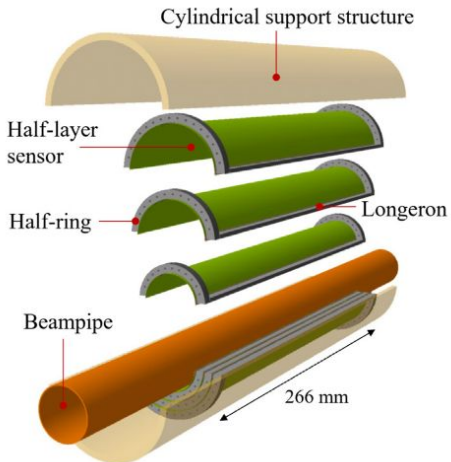


FoCal-E: high-granularity Si-W calorimeter for photons and π^0

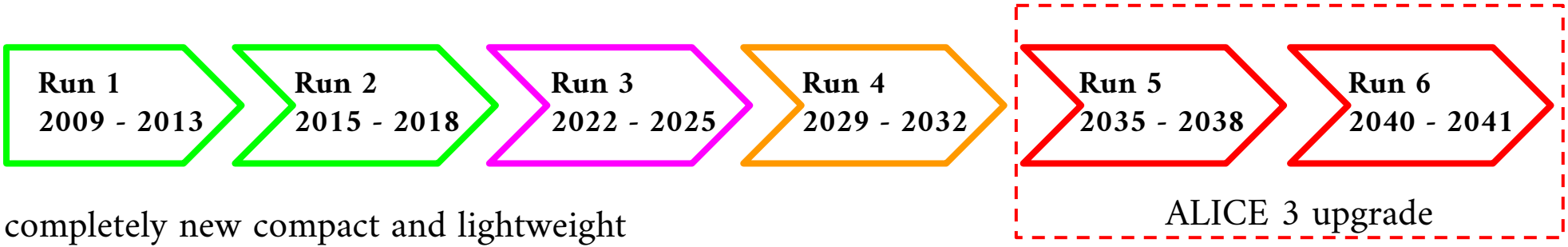
FoCal-H: hadronic calorimeter for photon isolation and jets

ITS3 (stitched wafer-scale monolithic sensors 65 nm CMOS technology.

- Replacement of 3 innermost layers of ITS2
- Curved wafer-scale ultra-thin silicon sensors:
  - low power / air cooling / less material
  - material budget: 0.05% X0 per layer
- High-precision, efficient low-pT tracking

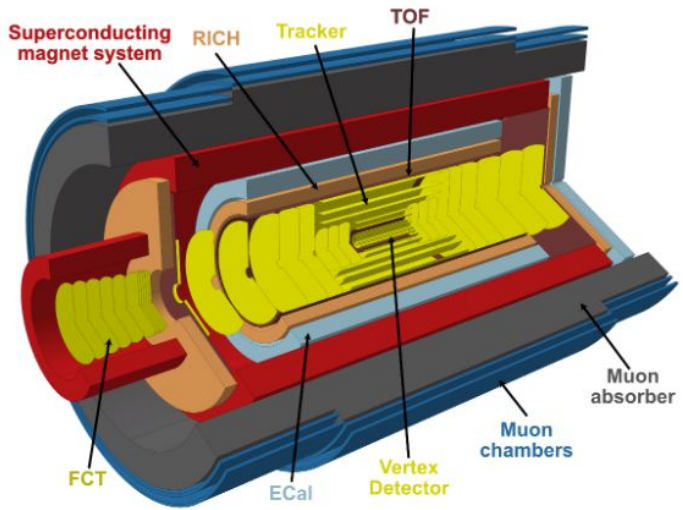


ALICE upgrades



A completely new compact and lightweight silicon based tracker

Run 5 and Run6 : pp, pA, AA (?)



High PID capabilities + low mass tracking system

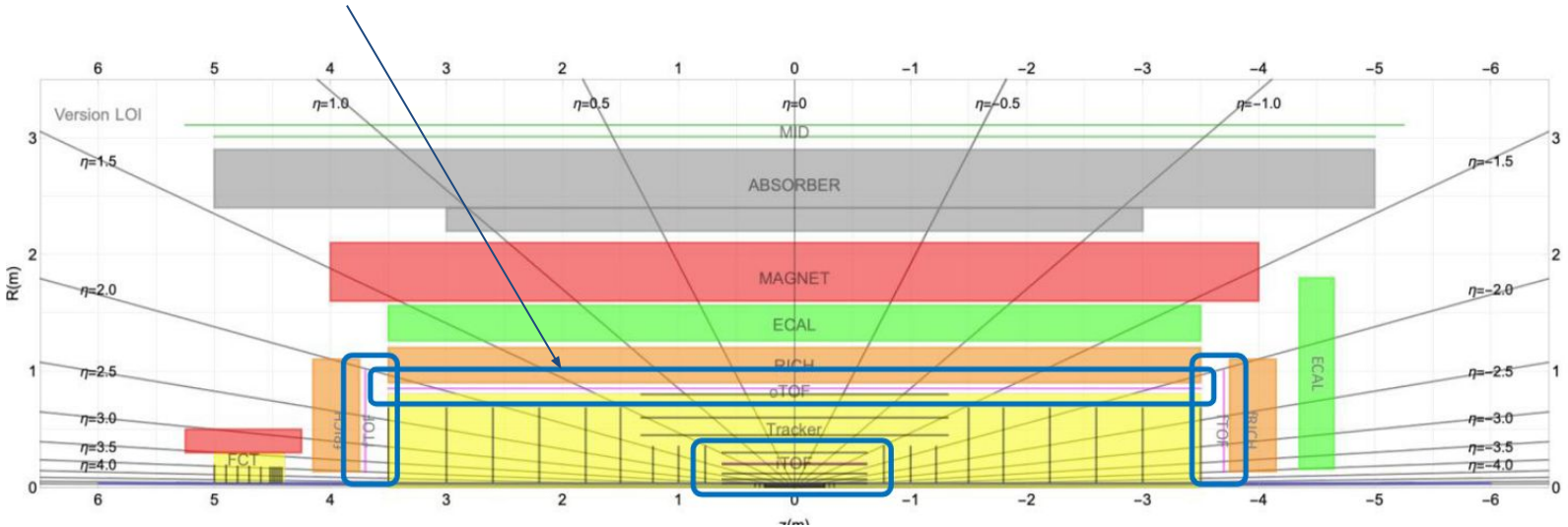
Covering a much larger rapidity range than the current ALICE setup Barrel ($|\eta| < 1.75$) Forward ($1.75 < |\eta| < 4$).

This provides an unique access to thermal dielectron production and heavy flavour probes of the quark–gluon plasma.

The ALICE 3 ToF layers

Particle identification over the full acceptance ($|\eta|< 4$)
2 barrel + 1 forward ToF layers:

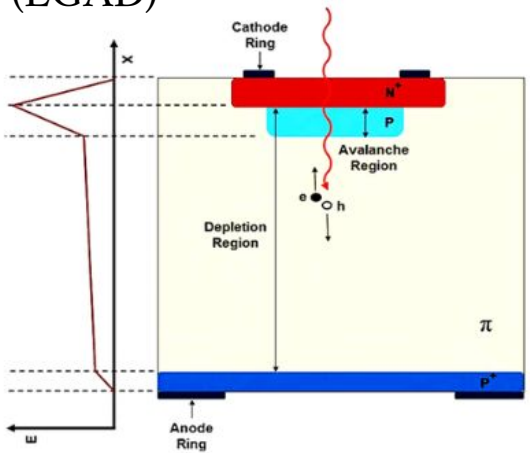
- Two layers → InnerTOF and OuterTOF located at 20 cm and 85 cm from the beam pipe (Barrel TOF $|\eta|<2$)



- Forward TOF located at 405 cm on either side of the interaction point (Forward TOF $2<|\eta|<4$)

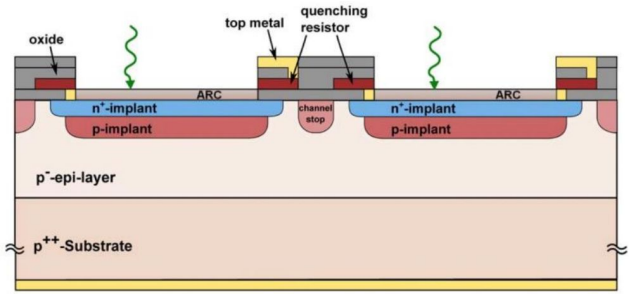
R&D for the Time of Flight system

Low Gain Avalanche Diode (LGAD)



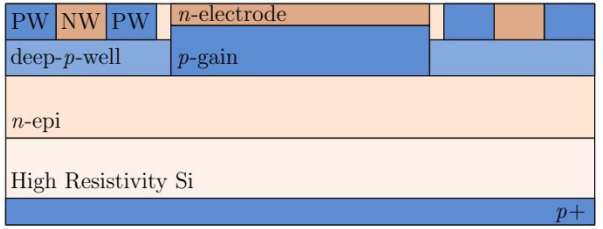
- Timing resolution of ~30 ps (50 µm thickness)
- Thinner sensors can be produced
- The dedicated readout electronics can increase drastically the price

Silicon Photomultiplier (SiPM)



- Timing resolution of ~40 ps for single photons detection.
- Very promising results on MIP detection (Beam test July 2024)
- Issues: Dark count / radiation hardness

CMOS Monolithic Active Pixel Sensor



- Low material budget
- Cheaper and easy assembly
- Low power consumption
- Investigation under progress (Beam test October 23/24)

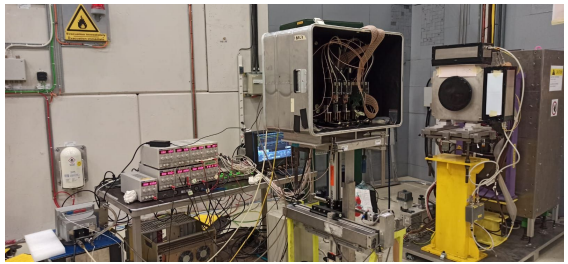
HEPIC participation in ALICE3 TOF

3 Beam test at PS:

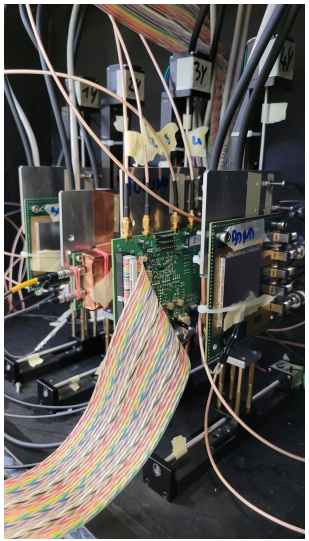
- October 2023 (focused mainly on the first CMOS design and on LGAD
- July 2024 (focused in the PicoTDC electronics for readout - SiPM with different coating layers - CMOS)
- October 2024 (starting tomorrow - I will join on friday - CMOS with corrected gain)

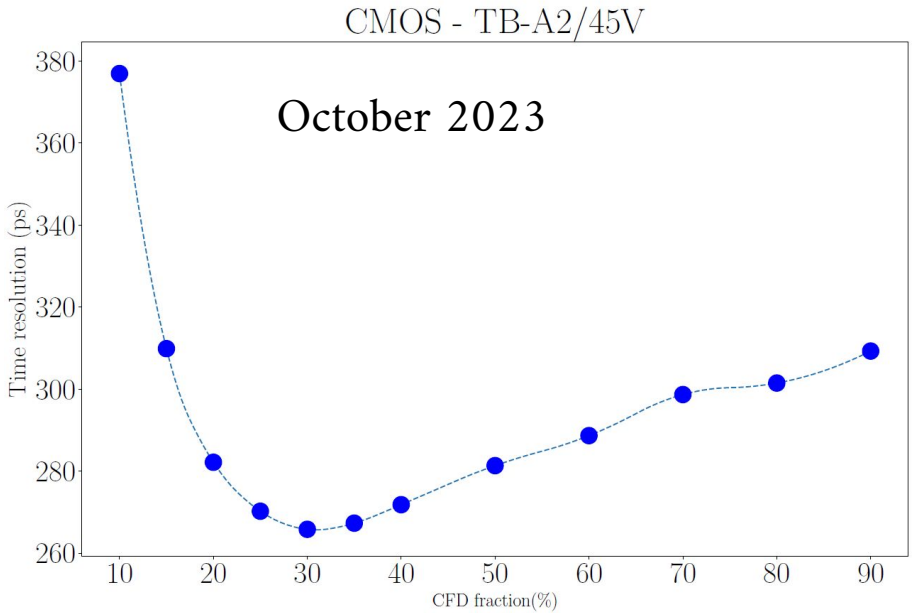
Participation in the data decoding for the PicoTDC / Analysis of the CMOS data

Article: https://doi.org/10.1088/1748-0221/19/07/P07033



Measurements of time resolution at CERN's PS (proton synchrotron) - 10 GeV/c





Thank you!
Questions?

Contact: geovane.souza@usp.br